Compal

EL5C3/EL531/EL431

DIS M/B Schematic Document

Intel Whiskey Lake Processor with DDR4

2018-09-20

LA-H101P

REV: 0.A (EVT)

Security Classification	Compal Secret Data		
Issued Date	2018/09/21	Deciphered Date	2019/09/21

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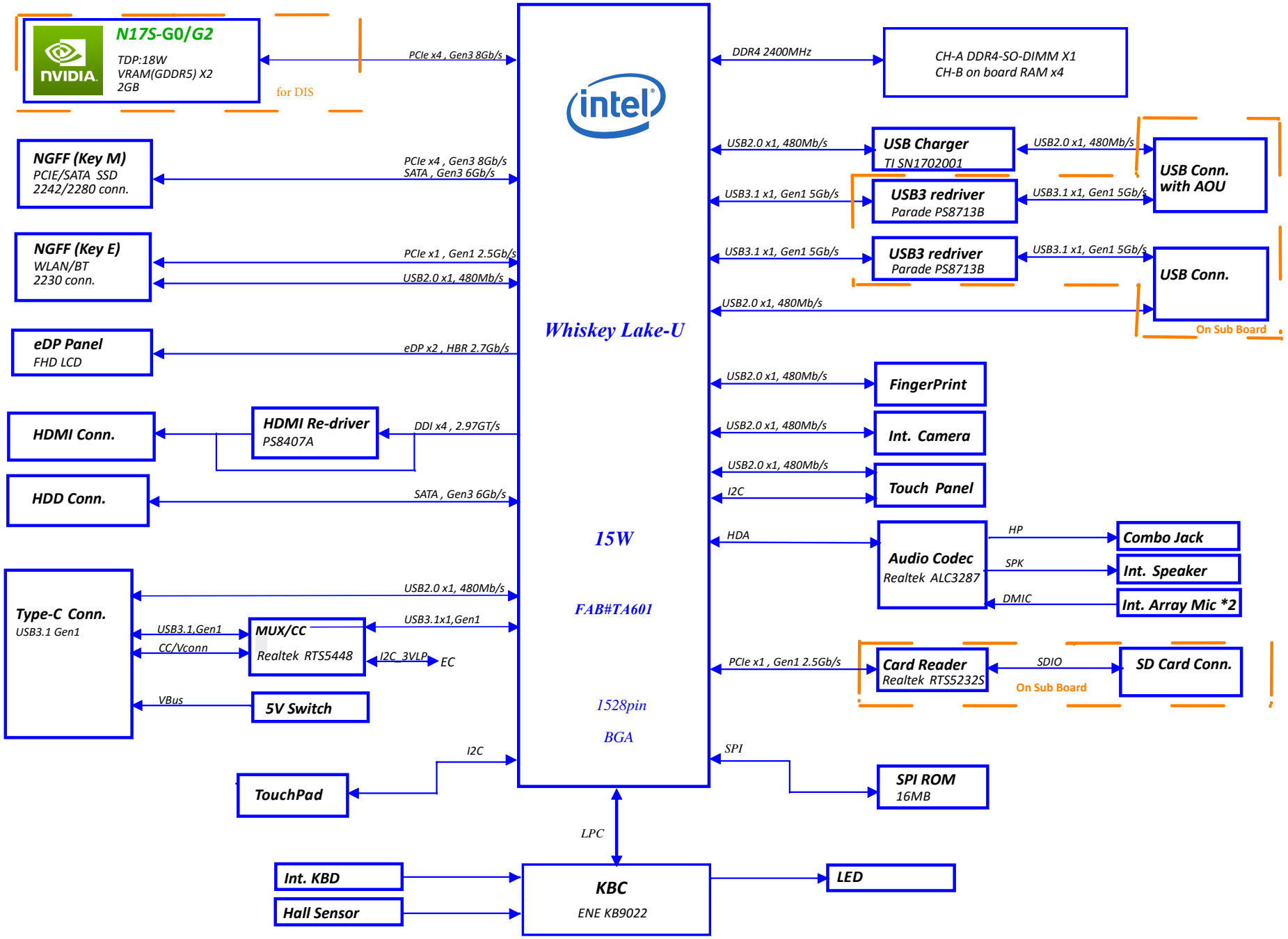

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Voltage Rails

power plane / State	B+	+5VALW +3VALW +1.8VALW +1.05VALW	+1.2V +2.5V	+5VS +3VS +VCCPLL_OC +1.05VS_VCCSTG +VCC_CORE +VCC_GT +VCC_SA +1.05V_VCCST +1.05VS_VCCIO +1.8VS +0.6VS
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

BOM Structure Table

Item	BOM Structure
DIS Only Components	DIS@
UMA Only Components	UMA@
HDMI Logo	45@
Touch Screen	TS@
Memory Down - SDP Package	SDP@
Memory Down - DDP Package	DDP@
GPU GC6 Components	GC6@
Un-Mount GPU GC6 Components	NOGC6@
Connectors	ME@
Intel CNVi	CNVi@
EMI Category	EMI@
ESD Category	ESD@
RF Category	RF@
Test Point	TP@
Keyboard BackLight	KBL@
	NOKBL@
Project select	S540@
	S340@
	C340@
	S340_14@
	S340_15@
GPU select	N17S_G1@
	N17S_G0@
	N16V@
	N16S@
	N16@
	N17@
Memory Down select	MD@
	NO_MD@
MIC select	Arrary_MIC@
	Single_MIC@
TypeC 20V_PRTCT	20V_PRTCT@

Item	BOM Structure
S340_15 MD (Hynix 4GB)	H4G_S340_15@
S340_15 MD (Micron 4GB)	M4G_S340_15@
S340_15 MD (Samsung 4GB)	S4G_S340_15@
C340 MD (Hynix 4GB)	H4G_C340@
C340 MD (Micron 4GB)	M4G_C340@
C340 MD (Samsung 4GB)	S4G_C340@
On Board RAM X76 Resistors	X76RAM@
S340_15@ VRAM (Hynix 2GB)	VH2G_S340_15@
S340_15@ VRAM (Micron 2GB)	VM2G_S340_15@
S340_15@ VRAM (Samsung 2GB)	VS2G_S340_15@
C340 VRAM (Hynix 2GB)	VH2G_C340@
C340 VRAM (Micron 2GB)	VM2G_C340@
C340 VRAM (Samsung 2GB)	VS2G_C340@
S340_14 MD (Hynix 4GB)	H4G_S340_14@
S340_14 MD (Micron 4GB)	M4G_S340_14@
S340_14 MD (Samsung 4GB)	S4G_S340_14@
S340_14@ VRAM (Hynix 2GB)	VH2G_S340_14@
S340_14@ VRAM (Micron 2GB)	VM2G_S340_14@
S340_14@ VRAM (Samsung 2GB)	VS2G_S340_14@

USB 2.0 Port Table

Port	External USB Port
1	USB2/3 Port (IO - 1)
2	USB2/3 Port (IO - 2)
3	USB2/3 Port (Type-C)
4	Touch Screen
5	
6	Camera
7	Fingrt Print
8	
9	
10	NGFF WLAN+BT

USB 3.0 Port Table

Port	
1	USB2/3 Port (IO - 1)
2	USB2/3 Port (IO - 2)
3	USB2/3 Port (Type-C)
4	
5	
6	

PCIE Port Table

Port	Lane	
1		
2		
3		
4	0	
5	0	
6	1	DGPU
7	2	
8	3	
9	1	CardReader
10	0	
11		NGFF WLAN+BT
12	0	
13	3	
14	2	SSD
15	1	
16	0	

SATA Port Table

Port	
0	
1A	HDD
1B	SSD1

EC SM Bus1 address

Device	Address
Smart Battery	0001 011x 16h

EC SM Bus2 address

Device	Address
NCT7718W	1001 100x 98h

PCH SM Bus address

Device	Address
DDR_JDIMM1 Touch Pad	1010 000x A0h

GPU SM Bus address

Device	Address
Internal thermal sensor	1001 111x 9Eh

SMBUS Control Table

	SOURCE	DGPU	BATT	CHARGER	NECP388	SODIMM	TP	PCH	G-SENSOR	THM sensor
EC_SMB_CK1 EC_SMB_DA1	NECP388 +3VL	X	V +3VALW	V +19V_VIN	X	X	X	X	X	X
EC_SMB_CK2 EC_SMB_DA2	NECP388 +3VS	V +3VS	X	X	V +3VS	X	X	V +3VS	X	V +3VS
EC_SMB_CK4 EC_SMB_DA4	NECP388 +3VS	X	X	X	X	X	X	X	V +3VS	X
SOC_SMBCLK SOC_SMBDATA	PCH +3VALW	X	X	X	X	V +3VS	V +3VS	X	X	X
SOC_SML0CLK SOC_SML0DATA	PCH +3VALW	X	X	X	X	X	X	X	X	X
EC_SMB_CK2 EC_SMB_DA2	PCH +3VS	V +3VS	X	X	V +3VS	X	X	X	X	X

SIGNAL / STATE	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

ON BOARD RAM * 4 (total 4GB)

C340

ZZZ H4G_C340@ — X76 HYNIX 4GB MD (X7680538LA1)
ZZZ M4G_C340@ — X76 MICRON 4GB MD (X7680538LA2)
ZZZ S4G_C340@ — X76 SAMSUNG 4GB MD (X7680538LA3)

S340-15

ZZZ H4G_S340_15@ — X76 HYNIX 4GB MD (X7680438L81)
ZZZ M4G_S340_15@ — X76 MICRON 4GB MD (X7680438L82)
ZZZ S4G_S340_15@ — X76 SAMSUNG 4GB MD (X7680438L83)

S340-14

ZZZ H4G_S340_14@ — X76 HYNIX 4GB MD (XXXXXXXXX)
ZZZ M4G_S340_14@ — X76 MICRON 4GB MD (XXXXXXXXX)
ZZZ S4G_S340_14@ — X76 SAMSUNG 4GB MD (XXXXXXXXX)

GPU

UV1 N17S_G0@ — N17S-G0-A1 (SA0000CC900)
UV1 N17S_G2@ — N17S-G2-A1 (SA0000CCB00)

WHL CPU

UC1 SRD1W i3_R1@ — i3-8145U (SA0000C6R20)
UC1 SREJQ i5_R1@ — i5-8265U (SA0000C6Q20)
UC1 SRFFW i7_R1@ — i7-8565U (SA0000C6P20)
UC1 SRFG1 Pentium 5405U@ — i3-8145U (SA0000C6R30)

PCB

ZZZ PCB@ — PCB (DA0001H6000)

X4E

S340-15 C340-14 S340-14

ZZZ S340_15@ — X4E S340-15 (X4EAF838L51)
ZZZ C340@ — X4E C340 (X4EAF838L01)
ZZZ1 S340_14@ — X4E S340-14 (XXXXXXXXXX)

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Title: Notes List

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-PowerMap_DDR4_Volume_NON CS]

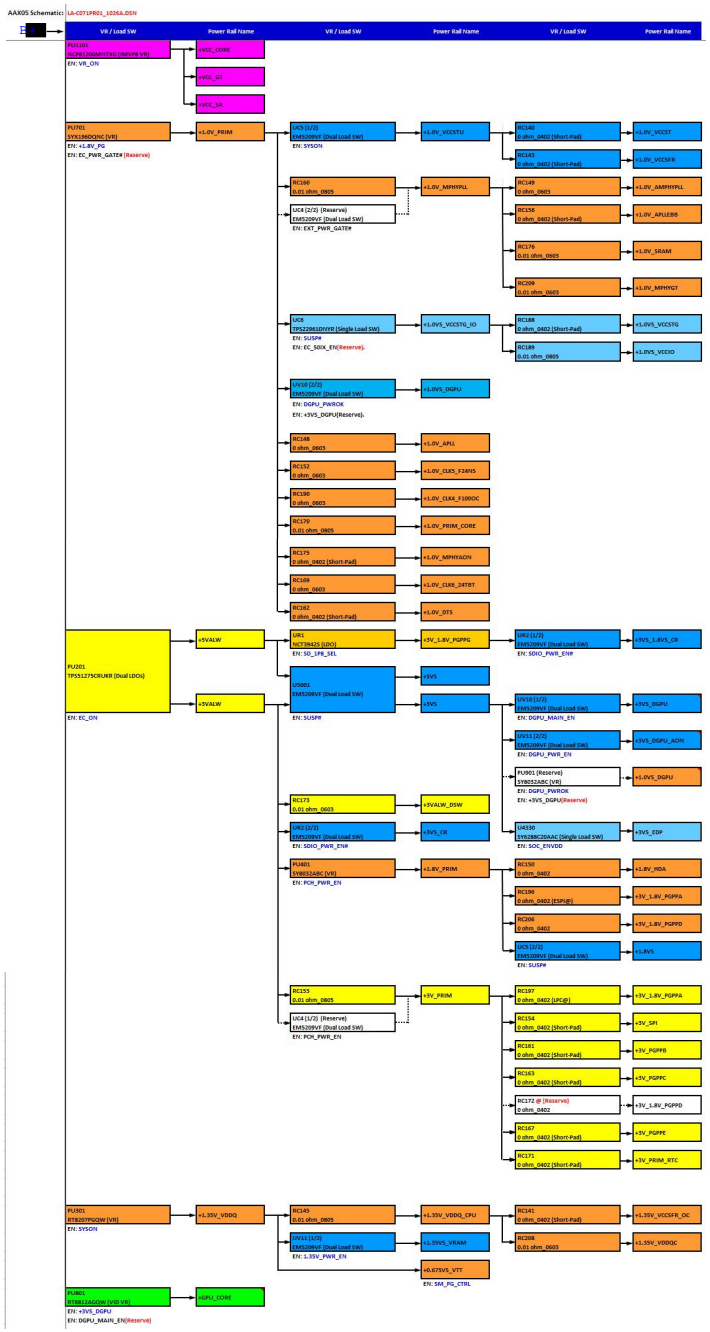

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Table 5-13. DDI Disabling and Termination Guidelines

Port	Strap	How to Enable Port?	How to Disable Port?
Port 1	DDPB_CTRLDATA	Pull up to 3.3 V with 2.2-k ohm ±5% resistor	No Connect
Port 2	DDPC_CTRLDATA	Pull up to 3.3 V with 2.2-k ohm ±5% resistor	
Port 3	DDPD_CTRLDATA	Pull up to 3.3 V with 2.2-k ohm ±5% resistor	
Port 4	DDPF_CTRLDATA	Pull up to 3.3 V with 2.2-k ohm ±5% resistor	

< Compensation PU For eDP >

+1.05VS_VCCIO

RC2 1 2 24.9_0201_1% EDP_COMP

Trace width=20 mils, Spacing=25mil, Max length=600mils

<HDMI>

<29> CPU_DP2_N0
<29> CPU_DP2_P0
<29> CPU_DP2_N1
<29> CPU_DP2_P1
<29> CPU_DP2_N2
<29> CPU_DP2_P2
<29> CPU_DP2_N3
<29> CPU_DP2_P3

HDMI DDC (Port 2)

<29,30> CPU_DP2_CTRL_CLK
<29,30> CPU_DP2_CTRL_DATA
<28> TS_I2C_RST#

UC1A

DDI1_TXN_0 AL5
DDI1_TXP_0 AL6
DDI1_TXN_1 AJ5
DDI1_TXP_1 AJ6
DDI1_TXN_2 AF6
DDI1_TXP_2 AF5
DDI1_TXN_3 AE5
DDI1_TXP_3 AE6

DDI2_TXN_0 AC4
DDI2_TXP_0 AC3
DDI2_TXN_1 AC1
DDI2_TXP_1 AC2
DDI2_TXN_2 AE4
DDI2_TXP_2 AE3
DDI2_TXN_3 AE1
DDI2_TXP_3 AE2

EDP_COMP AM6 DISP_RCOMP

GPP_E18/DPPB_CTRLCLK/CNV_BT_HOST_WAKE# CC8
GPP_E19/DPPB_CTRLDATA CC9

GPP_E20/DPPC_CTRLCLK CH4
GPP_E21/DPPC_CTRLDATA CH3

GPP_E22/DPPD_CTRLCLK CP4
GPP_E23/DPPD_CTRLDATA CN4

GPP_H16/DDPF_CTRLCLK CR26
GPP_H17/DDPF_CTRLDATA CP26

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EDP_TXN_0 AG4
EDP_TXP_0 AG3
EDP_TXN_1 AG2
EDP_TXP_1 AG1
EDP_TXN_2 AJ4
EDP_TXP_2 AJ3
EDP_TXN_3 AJ2
EDP_TXP_3 AJ1

EDP_TXN0 <28>
EDP_TXP0 <28>
EDP_TXN1 <28>
EDP_TXP1 <28>

<eDP>

EDP_AUX_N AH4
EDP_AUX_P AH3

EDP_AUXN <28>
EDP_AUXP <28>

DISP_UTILS AM7

DDI1_AUX_N AC7
DDI1_AUX_P AC6
DDI2_AUX_N AD4
DDI2_AUX_P AD3
DDI3_AUX_N AG7
DDI3_AUX_P AG6

+3VS

EC_SCI# RC1 1 2 10K_0402_5%

GPP_E13/DDPB_HPD0/DISP_MISC0 CN6
GPP_E14/DDPC_HPD1/DISP_MISC1 CM6
GPP_E15/DPPD_HPD2/DISP_MISC2 CP7
GPP_E16/DPPE_HPD3/DISP_MISC3 CP6
GPP_E17/EDP_HPD/DISP_MISC4 CM7

CPU_DP2_HPD <29,30>
EC_SCI# <34>
EDP_HPD <28>

From HDMI

EC_SCI#

CK11 EDP_BKLTEN
CG11 EDP_VDDEN
CH11 EDP_BKLTCTL

ENBKL <34>
PCH_ENVDD <28>
INVPWM <28>

From eDP

+1.05V_VCCST

RC8 1 2 1K_0402_5% H_THERMTRIP#

RC10 2 @ 1 49.9_0402_1% CATERR#

+1.05VS_VCCSTG

RC3 1K_0402_5%

<34> H_PROCHOT#

RC4 499_0402_1%

<34> H_PECI

If routed MS, PECI requires 18 mils spacing to other signals

CATERR# AA4
PECI AR1
PROCHOT# Y4
THRMTRIP# BJ1

H_PROCHOT#_R
H_THERMTRIP#

BPM#_0 U1
BPM#_1 U2
BPM#_2 U3
BPM#_3 U4

GPP_E3/CPU_GP0 CE9
GPP_E7/CPU_GP1 CN3
GPP_B3/CPU_GP2 CB34
GPP_B4/CPU_GP3 CC35

RC11 2 1 49.9_0402_1% CPU_POPIRCOMP BP27
RC12 2 1 49.9_0402_1% PCH_OPIRCOMP BW25
RC14 2 @ 1 49.9_0402_1% EDRAM_OPIO_RCOMP L5

RC15 2 @ 1 49.9_0402_1% EOPIO_RCOMP N5

PROC_POPIRCOMP
PCH_OPIRCOMP
OPCE_RCOMP

OPC_RCOMP

UC1D

PROC_TCK T6
PROC_TDI U6
PROC_TDO Y5
PROC_TMS T5
PROC_TRST# AB6

PCH_TCK W6
PCH_TDI U5
PCH_TDO W5
PCH_TMS P5
PCH_TRST# Y6
PCH_JTAGX P6

PROC_PREQ# W2
PROC_PRDY# W1

TP@ T1
TP@ T2

CPU_XDP_TCK0
SOC_XDP_TDI
SOC_XDP_TDO
SOC_XDP_TMS
SOC_XDP_TRST#

PCH_JTAG_TCK1
SOC_XDP_TDI
SOC_XDP_TDO
SOC_XDP_TMS
SOC_XDP_TRST#
CPU_XDP_TCK0

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< PU/PD for CMC Debug >

+1.05VS_VCCSTG

SOC_XDP_TMS RC5 1 CMC@ 2 51_0402_5%
SOC_XDP_TDI RC6 1 CMC@ 2 51_0402_5%
SOC_XDP_TDO RC7 1 DCI@ 2 51_0402_5%
CPU_XDP_TCK0 RC9 1 DCI@ 2 51_0402_5%
PCH_JTAG_TCK1 RC13 1 @ 2 51_0402_5%
SOC_XDP_TRST# RC16 1 @ 2 51_0402_5%

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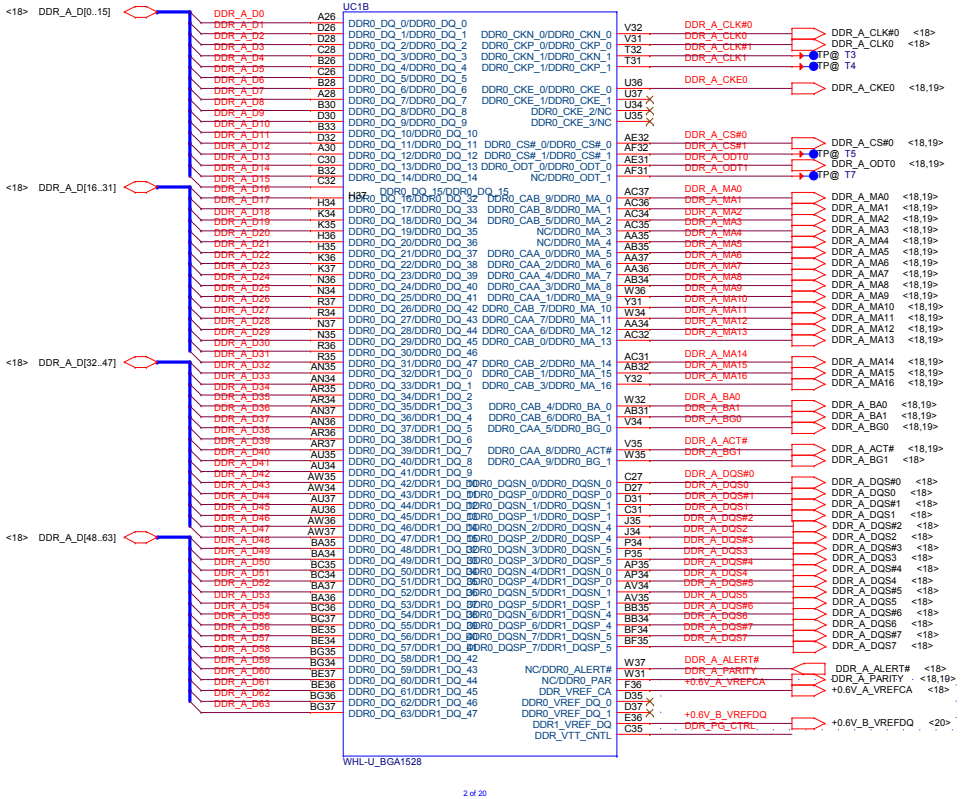
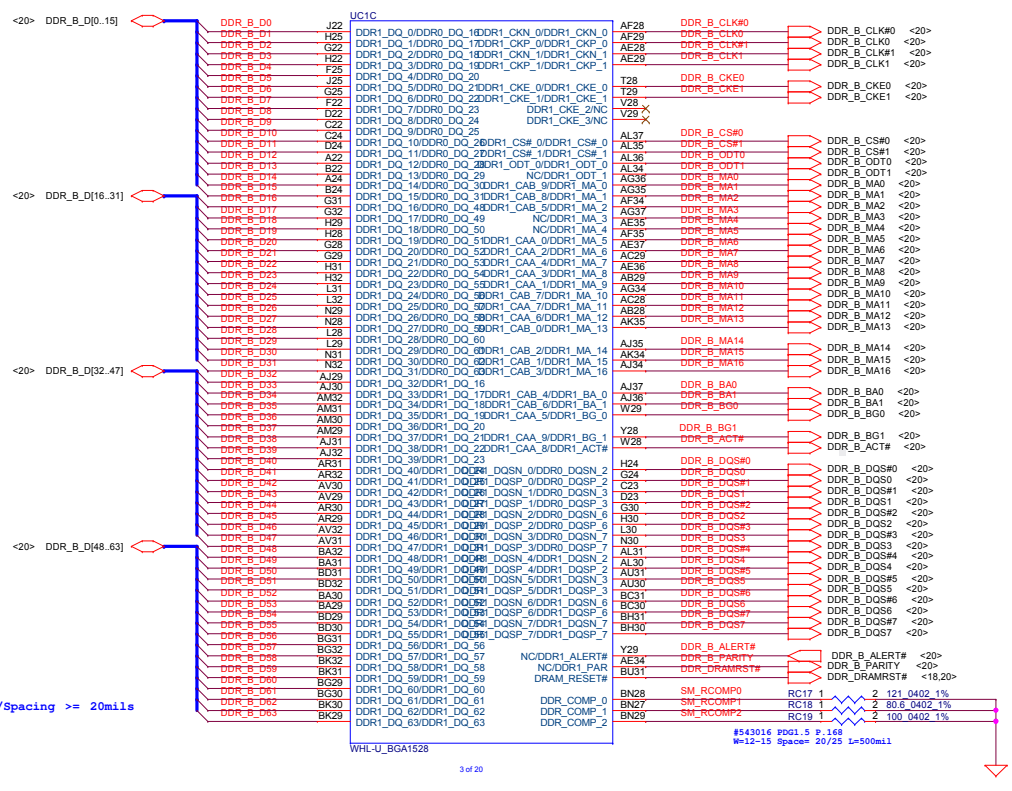
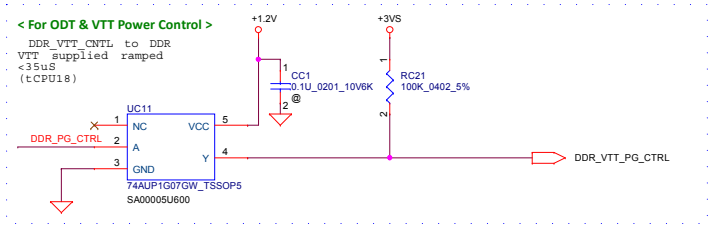
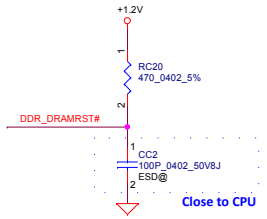
Interleaved Memory





Trace width/Spacing >= 20mils





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+3VALW

RC23 1 2 100K_0201_5% SOC_SPI_0_SI
RC24 1 2 100K_0201_5% SOC_SPI_0_IO2
RC25 1 2 100K_0201_5% SOC_SPI_0_IO3

Note: The internal pull-up is disabled when RSMRST# is asserted (during reset) and only enabled after RSMRST# de-assertion

SML1ALERT#/ PCHHOT#/GPP_B23	•If USB 3.1 Port 1 is used for 4-wire DCI.OOB (BSSB), and alternate functionality is also used on the pin, pull up to V3.3S with >100K resistor to avoid noise. •If USB 3.1 Port 1 is used for DCI.OOB (BSSB) 4-wire BSSB, and NO alternate functionality is used, leave float. •If DCI.OOB (BSSB) 2+2 functionality is used, pull up to V3.3S with a 4.7K resistor.

SML0ALERT# (Internal Pull Down):

eSPI or LPC

0 = LPC is selected for EC ==> Default

1 = eSPI is selected for EC

SPI ROM

UC1E

SOC_SPI_0_CLK CH37 — SPI0_CLK
SOC_SPI_0_SO CF37 — SPI0_MISO
SOC_SPI_0_SI CF36 — SPI0_MOSI
SOC_SPI_0_IO2 CF34 — SPI0_IO2
SOC_SPI_0_IO3 CG34 — SPI0_IO3
SOC_SPI_0_CS#0 CG36 — SPI0_CS0#
CG35 — SPI0_CS1#
CH34 — SPI0_CS2#

CF20 — GPP_D1/SPI1_CLK/BK1/SBK1
CG22 — GPP_D2/SPI1_MISO_IO1/BK2/SBK2
CF22 — GPP_D3/SPI1_MOSI_IO0/BK3/SBK3
CG23 — GPP_D21/SPI1_IO2
CH23 — GPP_D22/SPI1_IO3
CG20 — GPP_D0/SPI1_CS0#/BK0/SBK0

CH7 — CL_CLK
CH8 — CL_DATA
CH9 — CL_RST#

KB_RST# SERIRQ BV29 — GPP_A0/RCIN#/TIME_SYNC1
BV28 — GPP_A6/SERIRQ

GPP_C0/SMBCLK CK14 SOC_SMBCLK → SOC_SMBCLK <20>
GPP_C1/SMBDATA CH15 SOC_SMBDATA → SOC_SMBDATA <20>
GPP_C2/SMBALERT# CJ15 SOC_SMBALERT# → TP@ T8

GPP_C3/SML0CLK CH14 SOC_SML0CLK
GPP_C4/SML0DATA CF15 SOC_SML0DATA
GPP_C5/SML0ALERT# CG15 SOC_SML0ALERT# → TP@ T9

GPP_C6/SML1CLK CN15
GPP_C7/SML1DATA CM15 → EC_SMB_CK2 <34>, EC_SMB_DA2 <34>
GPP_B23/SML1ALERT#/PCHHOT# CC34 SOC_SML1ALERT#

GPP_A1/LAD0/ESPI_IO0 CA29 LPC_AD0 → LPC_AD0 <34>
GPP_A2/LAD1/ESPI_IO1 BY29 LPC_AD1 → LPC_AD1 <34>
GPP_A3/LAD2/ESPI_IO2 BY27 LPC_AD2 → LPC_AD2 <34>
GPP_A4/LAD3/ESPI_IO3 BV27 LPC_AD3 → LPC_AD3 <34>
GPP_A5/LFRAME#/ESPI_CS# CA28 LPC_FRAME# → LPC_FRAME# <34>
GPP_A14/SUS_STAT#/ESPI_RESET# CA27

GPP_A9/CLKOUT_LPC0/ESPI_CLK BV32 LPC_CLK0 RC27 1 EMI@ 2 22_0402_5% → CLK_LPC_EC <34>
GPP_A10/CLKOUT_LPC1 BV30
GPP_A8/CLKRUN# BY30 PM_CLKRUN# → PM_CLKRUN# <34>

WHL-U_BGA1528

SMB (Link to DDR)

SML1 (Link to EC, Thermal Sensor)

+3VS

RC26 1 2 10K_0402_5% KB_RST#

+3VS

RC28 1 2 8.2K_0402_5% SERIRQ

<34> SERIRQ

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close to SPI ROM

From SOC

SOC_SPI_0_SO RC29 1 2 33_0402_5% SOC_SPI_0_SO_R
SOC_SPI_0_CLK RC31 1 EMI@ 2 33_0402_5% SOC_SPI_0_CLK_R
SOC_SPI_0_SI RC32 1 2 33_0402_5% SOC_SPI_0_SI_R
SOC_SPI_0_IO3 RC34 1 2 33_0402_5% SOC_SPI_0_IO3_R

SOC_SPI_0_IO2 RC36 1 2 33_0402_5% SOC_SPI_0_IO2_R

From EC

<34> EC_SPI_CLK
<34> EC_SPI_MOSI
<34> EC_SPI_CS0#
<34> EC_SPI_MISO

EC_SPI_CLK RC41 1 EMI@ 2 33_0402_5% SOC_SPI_0_CLK_R
EC_SPI_MOSI RC42 1 2 33_0402_5% SOC_SPI_0_SI_R
EC_SPI_CS0# RC43 1 2 33_0402_5% SOC_SPI_0_CS#0
EC_SPI_MISO RC44 1 2 33_0402_5% SOC_SPI_0_SO_R

< SPI ROM - 16M >

+3VALW

CC3 1 @ 2 0.1U_0201_10V K X5R

UC12
SOC_SPI_0_CS#0 1 CS#
SOC_SPI_0_SO_R 2 DO(IO1)
SOC_SPI_0_IO2_R 3 IO2
4 GND
8 VCC
7 IO — SOC_SPI_0_IO3_R
6 CLK — SOC_SPI_0_CLK_R
5 DI(IO0) — SOC_SPI_0_SI_R

XM25QH128AHIG SOP 8P

CC4 @EMI@ 1 2 10P_0402_50V8J

+3VS

EC_SMB_CK2 RC30 1 2 1K_0402_5%
EC_SMB_DA2 RC33 1 2 1K_0402_5%

SOC_SML1ALERT# RC35 1 @ 2 150K_0402_5%

SOC_SMBCLK RC37 1 2 1K_0402_5%
SOC_SMBDATA RC38 1 2 1K_0402_5%
SOC_SML0CLK RC39 1 2 1K_0402_5%
SOC_SML0DATA RC40 1 2 1K_0402_5%

PM_CLKRUN# RC45 1 2 8.2K_0402_5%

Security Classification	Compal Secret Data		
Issued Date	2018/09/21	Deciphered Date	2019/09/21

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Compal Electronics, Inc.

Title: **WHL-U(3/12)SPI,SMB,LPC,ESPI**

Size: Custom | Document Number: **LA-H101P** | Rev: 0.A

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< HD AUDIO >

<33> HDA_BIT_CLK_R — RC46 1 EMI@ 2 33_0402_5% — HDA_BIT_CLK
<33> HDA_SYNC_R — RC48 1 2 33_0402_5% — HDA_SYNC
<33> HDA_SDOUT_R — RC47 1 2 33_0402_5% — HDA_SDOUT
HDA_SDOUT — RC49 499_0402_1% (1, @, 2)

< To Enable ME Override >

<34> ME_EN — RC51 1 @ 2 0_0402_5% — HDA_SDOUT

+3VS — RC55 1 @ 2 2.2K_0402_5% — HDA_SPKR

SPKR (Internal Pull Down):

TOP Swap Override

0 = Disable TOP Swap mode. ==> Default

1 = Enable TOP Swap Mode.

75K_0402_5% 1 CNVi@ 2 RC52 — CNV_RF_RESET#

Follow Jefferson Peak schematic check list.

RC164 1 @ 2 1K_0402_5% — WLBT_OFF#

TO DGPU

SOC_GPIO_C10 — RC59 1 @ 2 0_0402_5% — GPU_EVENT# — GPU_EVENT# [24]

UC1G

HDA_SYNC	BN34	HDA_SYNC/I2S0_SFRM	
HDA_BIT_CLK	BN37	HDA_BCLK/I2S0_SCLK	
HDA_SDOUT	BN36	HDA_SDO/I2S0_TXD	
<33> HDA_SDIN0	BN35	HDA_SDI0/I2S0_RXD	
	BL36	HDA_SDI1/I2S1_RXD/SNDW1_DATA	GPP_G0/SD_CMD CH36
	BL35	HDA_RST#/I2S1_SCLK/SNDW1_CLK	GPP_G1/SD3_DATA0 CL35
	CK23	GPP_D23/I2S_MCLK	GPP_G2/SD3_DATA1 CL36
	BL37	I2S1_SFRM/SNDW2_CLK	GPP_G3/SD3_DATA2 CM35
	BL34	I2S1_TXD/SNDW2_DATA	GPP_G4/SD_DATA3 CN35
			GPP_G5/SD_CD# CH35
			GPP_G6/SD_CLK CK36
			GPP_G7/SD_WP CK34
<31> CNV_RF_RESET#	CNV_RF_RESET# CJ32	GPP_H1/I2S2_SFRM/CNV_BT_I2S_BCLK/CNV_RF_RESET#	
<31> CLKREQ_CNV#	CH32	GPP_H0/I2S2_SCLK/CNV_BT_I2S_SCLK	
	CH29	GPP_H2/I2S2_TXD/CNV_BT_I2S_SDI/MODEM_CLKREQ	
	CH30	GPP_H3/I2S2_RXD/CNV_BT_I2S_SDO	GPP_A17/SD_VDD1_PWR_EN#/ISH_GP7 BW36
			GPP_A16/SD_1P8_SEL BY31
	CP24	GPP_D19/DMIC_CLK0/SNDW4_CLK	
	CN24	GPP_D20/DMIC_DATA0/SNDW4_DATA	
			SD_1P8_RCOMP CK33
	CK25	GPP_D17/DMIC_CLK1/SNDW3_CLK	SD_3P3_RCOMP CM34 — SOC_SD_RCOMP — RC50 1 2 200_0402_1%
	CJ25	GPP_D18/DMIC_DATA1/SNDW3_DATA	
<33> HDA_SPKR	HDA_SPKR CF35	GPP_B14/SPKR	

WHL-U_BGA1528

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GPP_H21 XTAL frequency select.
0: 38.4 / 19.2 MHz
1: 24MHz XTAL select.

UC1I

<31> CNV_CRX_DTX_N0	CR30	CNV_WR_D0N	GPP_H18/CPU_C10_GATE# CN27 — SOC_C10_GATE# — TP@ T10
<31> CNV_CRX_DTX_P0	CP30	CNV_WR_D0P	GPP_H19/TIMESYNC_0 CM27
<31> CNV_CRX_DTX_N1	CM30	CNV_WR_D1N	GPP_H21 CF25 — SOC_GPP_H21 — RC53 1 2 4.7K_0201_5%
<31> CNV_CRX_DTX_P1	CN30	CNV_WR_D1P	GPP_H22 CN26
<31> CNV_CTX_DRX_N0	CN32	CNV_WT_D0N	GPP_H23 CM26
<31> CNV_CTX_DRX_P0	CM32	CNV_WT_D0P	GPP_F10 CK17
<31> CNV_CTX_DRX_N1	CP33	CNV_WT_D1N	GPD7 BV35 — SOC_GPD7 — RC54 1 2 100K_0201_5%
<31> CNV_CTX_DRX_P1	CN33	CNV_WT_D1P	GPP_F3 CN20
<31> CLK_CNV_CRX_DTX_N	CN31	CNV_WR_CLKN	GPP_D4/IMGCLKOUT0/BK4/SBK4 CG25
<31> CLK_CNV_CRX_DTX_P	CP31	CNV_WR_CLKP	GPP_H20/IMGCLKOUT_1 CH25
<31> CLK_CNV_CTX_DRX_N	CP34	CNV_WT_CLKN	GPP_F12/EMMC_DATA0 CR20
<31> CLK_CNV_CTX_DRX_P	CN34	CNV_WT_CLKP	GPP_F13/EMMC_DATA1 CM20
RC56 1 CNVi@ 2 — CNV_WT_RCOMP	CP32	CNV_WT_RCOMP_0	GPP_F14/EMMC_DATA2 CN19
150_0402_1%	CR32	CNV_WT_RCOMP_1	GPP_F15/EMMC_DATA3 CM19
	CP20	GPP_F0/CNV_PA_BLANKING	GPP_F16/EMMC_DATA4 CN18
For MX230 [11] GC6_FB_EN1V8	GC6_FB_EN1V8 CK19	GPP_F1	GPP_F17/EMMC_DATA5 CR18
	CG17	GPP_F2	GPP_F18/EMMC_DATA6 CP18
<35> TP_INT#	CR14	GPP_C8/UART0_RXD	GPP_F19/EMMC_DATA7 CM18
	CP14	GPP_C9/UART0_TXD	
	CN14	GPP_C10/UART0_RTS#	GPP_F20/EMMC_RCLK CM16
<31> WLBT_OFF#	WLBT_OFF# CM14	GPP_C11/UART0_CTS#	GPP_F21/EMMC_CLK CP16
			GPP_F11/EMMC_CMD CR16
	CJ17		GPP_F22/EMMC_RESET# CN16
	CH17	GPP_F8/CNV_MFUART2_RXD	
RC57 1 2 SOC_A4WP_PRESENT	CF17	GPP_F9/CNV_MFUART2_TXD	EMMC_RCOMP CK15 — SOC_SD_RCOMP
10K_0402_5%		GPP_F23/A4WP_PRESENT	

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+3VALW

XTAL INPUT MODE (HVM ONLY)
LOW: XTAL INPUT IS SINGLE ENDED
HIGH: XTAL IS ATTACHED

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Issued Date	2018/09/21	Deciphered Date	2019/09/21

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Compal Electronics, Inc.

Title: WHL-U(4/12)HDA,EMMC,SDIO,CSI2

Size: Custom | Document Number: LA-H101P | Rev: 0.A

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SRCCLKREQ#[5:0].

Any used, enabled, and mapped SRCCLKREQ# signal should connect to a PCIe* connector pin or a device down ball with a 10K Ohm ±10% external pull-up resistor to core rail..

Any un-used, disabled, and non-mapped SRCCLKREQ# signal must be left as no connects at the PCH side on the platform..

Note: The SRCCLKREQ# signals can be configured to map to any of the PCH PCI Express* Root Ports while using any of the CLKOUT_PCIE_P/N differential pairs. Refer to latest version of the Cannon Lake PCH External Design Specification (EDS) and Intel® PW Bring-Up Guide for details on how to assign the SRCCLKREQ# signals..

5/9 Naming Rule

+3VS

RC61 1 2 10K_0402_5% CLKREQ_PCIE#1
RC63 1 2 10K_0402_5% CLKREQ_PCIE#3
RC64 1 2 10K_0402_5% CLKREQ_PCIE#4
RC68 1 @ 2 10K_0402_5%

DGPU [21] CLK_PEG_N0 [21] CLK_PEG_P0 [21] CLKREQ_PEG#0
SSD <32> CLK_PCIE_N1 <32> CLK_PCIE_P1 <32> CLKREQ_PCIE#1
WLAN <31> CLK_PCIE_N3 <31> CLK_PCIE_P3 <31> CLKREQ_PCIE#3
Card Reader <37> CLK_PCIE_N4 <37> CLK_PCIE_P4 <37> CLKREQ_PCIE#4

UC1J

AW2 CLKOUT_PCIE_N_0 GPP_B5/SRCCLKREQ0# CLKREQ_PEG#0
AY3 CLKOUT_PCIE_P_0
CF32
BC1 CLKOUT_PCIE_N_1 GPP_B6/SRCCLKREQ1# CLKREQ_PCIE#1
BC2 CLKOUT_PCIE_P_1
CE32
BD3 CLKOUT_PCIE_N_2 GPP_B7/SRCCLKREQ2#
BC3 CLKOUT_PCIE_P_2
CF30
BH3 CLKOUT_PCIE_N_3 GPP_B8/SRCCLKREQ3# CLKREQ_PCIE#3
BH4 CLKOUT_PCIE_P_3
CE31
BA1 CLKOUT_PCIE_N_4 GPP_B9/SRCCLKREQ4# CLKREQ_PCIE#4
BA2 CLKOUT_PCIE_P_4
CE30
BE1 CLKOUT_PCIE_N_5 GPP_B10/SRCCLKREQ5#
BE2 CLKOUT_PCIE_P_5
CF31

AU1 CLKOUT_ITPXDP_N
AU2 CLKOUT_ITPXDP_P
BT32 GPD8/SUSCLK → SUSCLK <31>
CK3 XTAL_IN 33E_SOC_XTAL24_IN_R
CK2 XTAL_OUT 33E_SOC_XTAL24_OUT_R
CJ1 CLK_BIASREF XCLK_BIASREF
CM3 CLKIN_XTAL CLKIN_XTAL → CLKIN_XTAL <31>
BN31 RTCX1 SOC_RTCX1
BN32 RTCX2 SOC_RTCX2
BR37 SRTCRST# SOC_SRTCRST#
BR34 RTCRST# SOC_RTCRST#

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XCLK_BIASREF RC60 1 2 60.4_0402_1%
CLKIN_XTAL RC65 1 2 10K_0402_5%

Follow CFL-U PDG_Rev_0.7
Stuff 60.4 ohm(RC110) PD for CNL-U/ WHL-U and CFL-U

33E_SOC_XTAL24_IN_R RC69 1 2 EMI@ 33_0201_5% 33E_SOC_XTAL24_IN
LC1 @EMI@ DLM0NSN900HY2D_4P
33E_SOC_XTAL24_OUT_R RC73 1 2 EMI@ 33_0201_5% 33E_SOC_XTAL24_OUT

RC74 1 2 200K_0402_1%

YC1 24MHZ_18PF_XRCGB24M000F2P51R0 SJ10000UJ00
NC NC
CC7 27P_0402_50V8J
CC8 27P_0402_50V8J

+3VL_RTC

RC70 1 2 20K_0402_5% SOC_SRTCRST#
CC5 1 2 1U_0201_6.3V6M SE00000UC00
RC71 1 2 20K_0402_5% SOC_RTCRST#
RC72 1 @ 2 0_0402_5% EC_CLEAR_CMOS# <34>
CC6 1 2 1U_0201_6.3V6M SE00000UC00
CLRP1 1 2 SHORT PADS CLR_CMOS
RC75 1 2 1M_0402_5% SM_INTRUDER#

< PCH PLTRST Buffer >

SOC_PLTRST# RC76 1 2 0_0402_5% PCI_RST# <31,32,34,37>
RC80 100K_0402_5%
CC9 ESD@ 100P_0402_50V8J

+3VALW

RC77 1 2 10K_0402_5% SYS_RESET#
RC78 1 2 10K_0402_5% PCH_PWROK
RC79 1 2 10K_0402_5% EC_RSMRST#

ESD@ CC10 100P_0402_50V8J SYS_RESET#
ESD@ CC11 100P_0402_50V8J EC_RSMRST#
ESD@ CC12 100P_0402_50V8J SYS_PWROK

SOC_RTCX2
SOC_RTCX1
RC81 1 2 10M_0402_5%
YC2 32.768KHZ_9PF_X1A000141000200 SJ10000PW00
CC13 8.2P_0402_50V8B
CC14 8.2P_0402_50V8B

+3VALW
RC82 1 2 1K_0402_5% WAKE#

UC1K

SOC_PLTRST# BJ35 GPP_B13/PLTRST#
SYS_RESET# CN10 GPP_B14/SYS_RESET#
EC_RSMRST# BR36 RSMRST#
<34> EC_RSMRST#
T11 TP@
H_CPUPWRGD AR2 PROCPWRGD
EC_VCCST_PG BJ2 VCCST_PWRGOOD
SYS_PWROK CR10 PCH_PWROK
PCH_PWROK DSW_PWROK
EC_RSMRST# BP30
<34> SYS_PWROK
<34> PCH_PWROK
BV34 GPP_A13/SUSWARN#/SUSPWRDACK
BY32 GPP_A15/SUSACK#
WAKE# BU30 WAKE#
BU32 GPD2/LAN_WAKE#
BU34 GPD11/LANPHYPC

GPP_B12/SLP_S0# BJ37 PM_SLP_S0# → TP@T12
GPD4/SLP_S3# BU36 PM_SLP_S3# → TP@T12 PM_SLP_S3# <34>
GPD5/SLP_S4# BU27 PM_SLP_S4# → TP@T13 PM_SLP_S4# <34,42,45>
GPD10/SLP_S5# BT29 PM_SLP_S5# → TP@T13
SLP_SUS# BU29
SLP_LAN# BT31
GPD9/SLP_WLAN# BT30 SLP_WLAN# → TP@T14
GPD6/SLP_A# BU37 PM_SLP_A# → TP@T15
GPD3/PWRBTN# BU28 PBTN_OUT#
GPD1/ACPRESENT BU35 AC_PRESENT_R RC83 1 @ 2 0_0402_5% PBTN_OUT# <34> AC_PRESENT <34>
GPD0/BATLOW# BV36 PM_BATLOW#
INTRUDER# BR35 SM_INTRUDER#
GPP_B11/EXT_PWR_GATE# CC37
GPP_B2/VRALERT# CC36 SOC_VRALERT#
INPUT3VSEL BT27 SOC_INPUT3VSEL

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+3VALW
PM_BATLOW# RC84 1 2 8.2K_0402_5%
AC_PRESENT RC85 1 @ 2 10K_0402_5%
SOC_VRALERT# RC86 1 @ 2 10K_0402_5%
SOC_INPUT3VSEL RC87 1 @ 2 4.7K_0402_5%
RC88 1 2 4.7K_0402_5%

From EC (Open-Drain)

+1.05V_VCCST
RC89 1K_0402_5%
<34> VCCST_PWRGD
RC90 1 2 60.4_0402_1% EC_VCCST_PG
CC15 100P_0402_50V8J ESD@

INPUT3VSEL	I	Strapped high if PCH's VCCDSW_3P3 rail is 3.0V +/-5%; else PCH's VCCDSW_3P3 rail is 3.3V +/- 5%. This pin is in the VCCPRIM_3P3 well. **Note:** When strapped for 3.0V operation, it is expected that the rest of the platform's 3.3V rails are at 3.0V (e.g. the battery is a 1S configured battery) and that components can function properly at 3.0V.

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Security Classification	Compal Secret Data		
Issued Date	2018/09/21	Deciphered Date	2019/09/21

Compal Electronics, Inc.

Title: WHL-U(5/12)CLK,PM,GPIO

Size: Custom | Document Number: LA-H101P | Rev: 0.A

Date: Thursday, September 20, 2018 | Sheet 10 of 51

GSPI0_MOSI (Internal Pull Down):

No Reboot

0 = Disable No Reboot mode. ==> Default

1 = Enable No Reboot Mode. (PCH will disable the TCO Timer system reboot feature). This funct i ons usef ul when running ITP/XDP.

GSPI1_MOSI (Internal Pull Down):

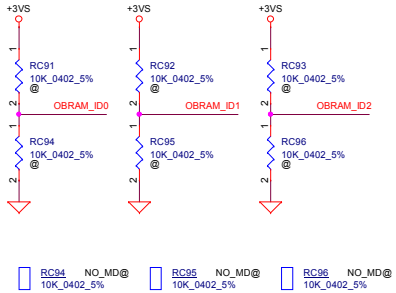
Boot BIOS Strap Bit

0 = SPI Mode ==> Default

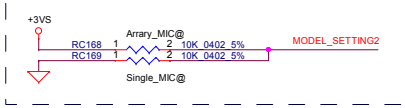
1 = LPC Mode

Capacity	Description	X76	PART NUMBER (R1)
4GB	WITHOUT ON-BOARD RAM	NO_MD@	N/A
	HYNIX 2666MHz (H5AN8G6NCJR-VKC) S340	X7680438L81	SA0000BMN00
	HYNIX 2666MHz (H5AN8G6NCJR-VKC) C340	X7680538LA1	
	MICRON 2666MHz (MT40A512M16LY-075:E) S340	X7680438L82	SA0000ARD20
	MICRON 2666MHz (MT40A512M16LY-075:E) C340	X7680538LA2	
	SAMSUNG 2666MHz (K4A8G165WC-BCTD) S340	X7680438L83	SA0000B6F00
	SAMSUNG 2666MHz (K4A8G165WC-BCTD) C340	X7680538LA3	
	N/A	N/A	N/A

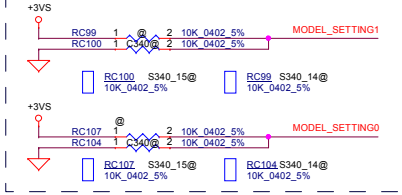
Capacity	Description	GPP_B19	GPP_B20	GPP_B21
		OBRAM_ID0	OBRAM_ID1	OBRAM_ID2
4GB	WITHOUT ON-BOARD RAM	0	0	0
	SAMSUNG 2666MHz (K4A8G165WC-BCTD)	0	0	1
	HYNIX 2666MHz (H5AN8G6NCJR-VKC)	0	1	0
	MICRON 2666MHz (MT40A512M16LY-075:E)	0	1	1
	N/A	1	0	0
	N/A	1	0	1
	N/A	1	1	0
	N/A	1	1	1



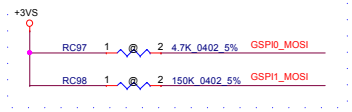
Function	MODEL_SETTING2 (GPP_D10)
Arrary MIC	1
Single MIC	0



Function	MODEL_SETTING1 (GPP_D12)	MODEL_SETTING0 (GPP_D11)
C340-15	0	0
S340-15	0	1
S340-14	1	0



Function	DGPU_PRSNT (GPP_C15)
DIS	0
UMA Only	1



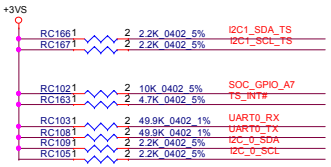
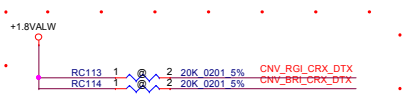
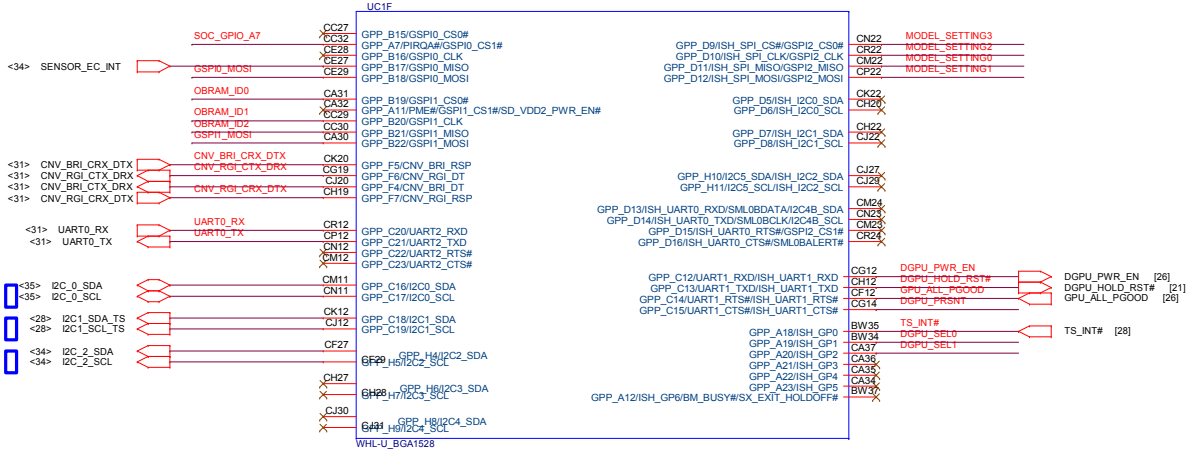


Table 1-26 Miscellaneous Signals on the Processor Checklist

Pin Name	System Pull-up / Pull-down	Schematics Notes	✓
RCIN#/GPP_A0	Pull-up to V3.3S with 10 KΩ resistor.	Driven by discrete glue logic or SIO which act as keyboard controller to generate INIT# to the processor.	
PROCPWRGD		This signal is indication of PROCPWRGOOD.	
PIRQA#/GPP_A7	Pull-up to V3.3S with 8.2 KΩ ~10 KΩ resistor.		

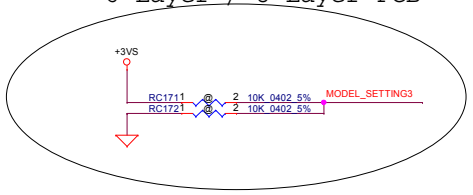


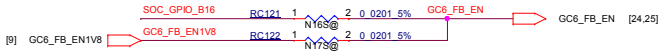
Place close to PCH



for RMT test

6 Layer / 8 Layer PCB





TO DGPU

Security Classification	Compal Secret Data		
Issued Date	2018/09/21	Deciphered Date	2019/09/21

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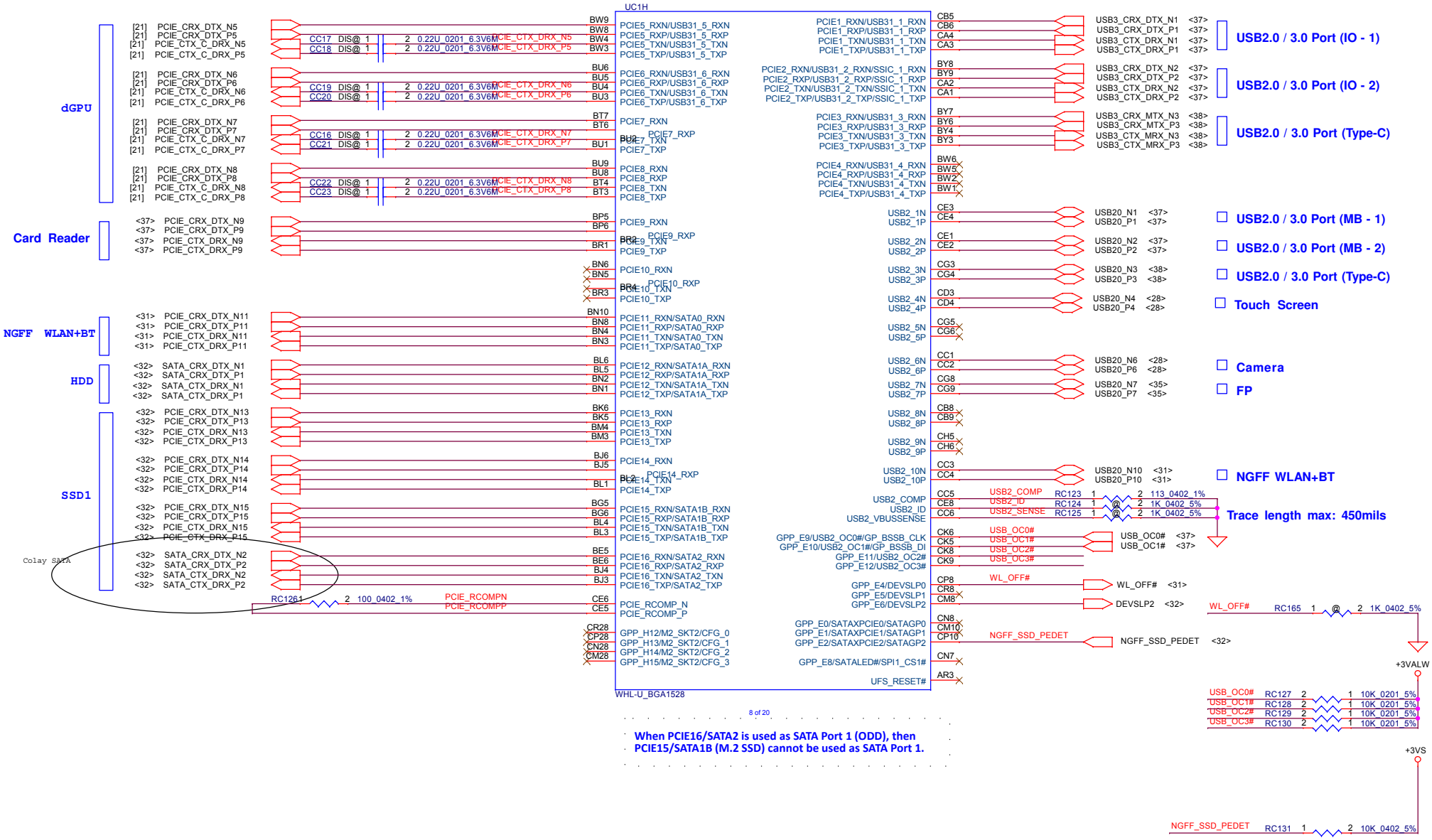
Compal Electronics, Inc.

Title: WHL-U(6/12)GPIO,I2C,GSPI

Size: Custom | Document Number: LA-H101P | Rev: 0.A

Date: Thursday, September 20, 2018 | Sheet 11 of 51



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Issued Date	2018/09/21	Deciphered Date	2019/09/21

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Compal Electronics, Inc.			
Title	WHL-U(7/12)PCIE,USB,SATA		
Size: Custom	Document Number: LA-H101P		Rev: 0.A
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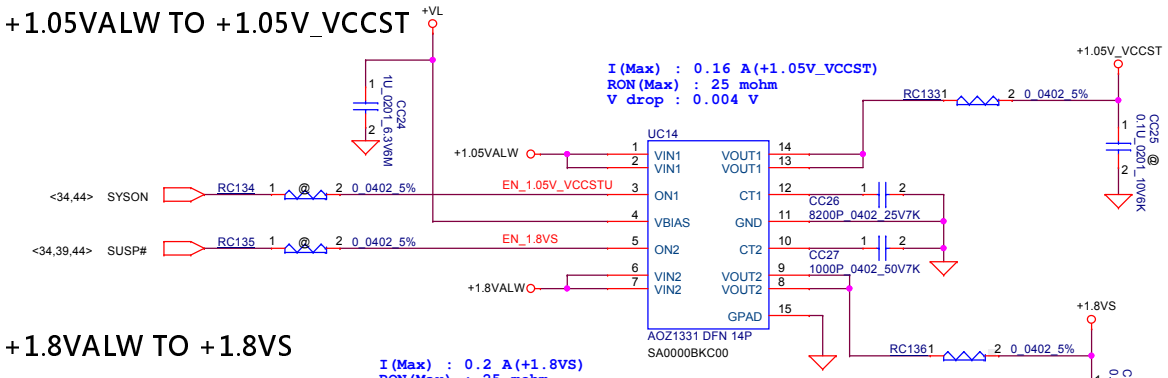
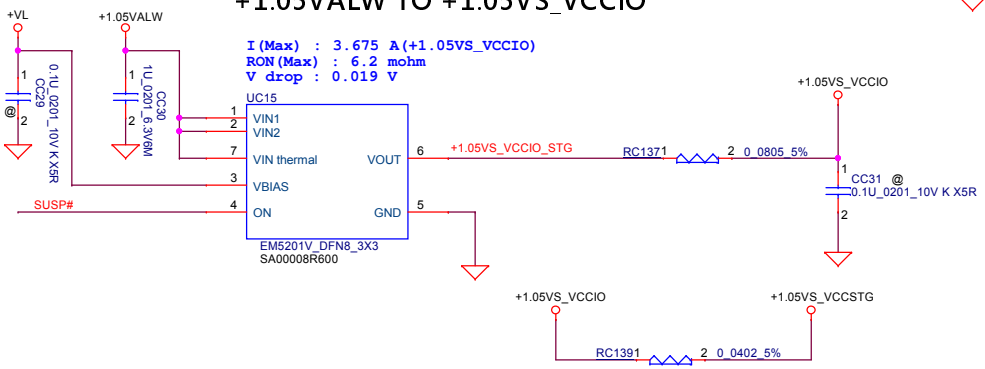
+1.05VALW TO +1.05V_VCCST

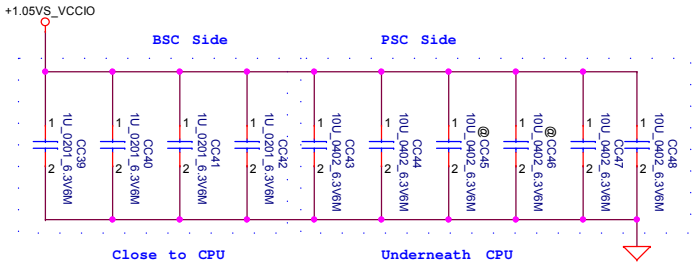


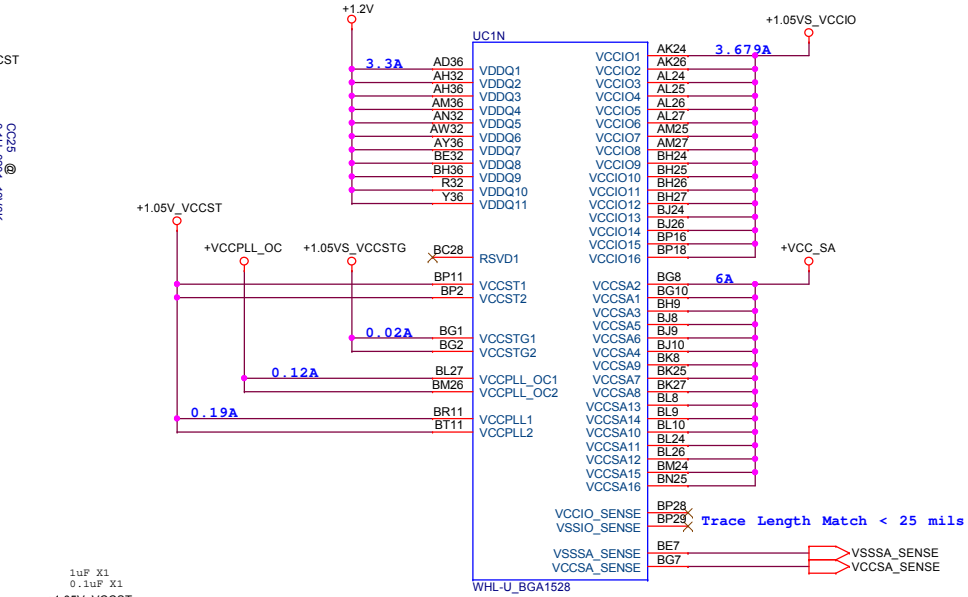
+1.8VALW TO +1.8VS

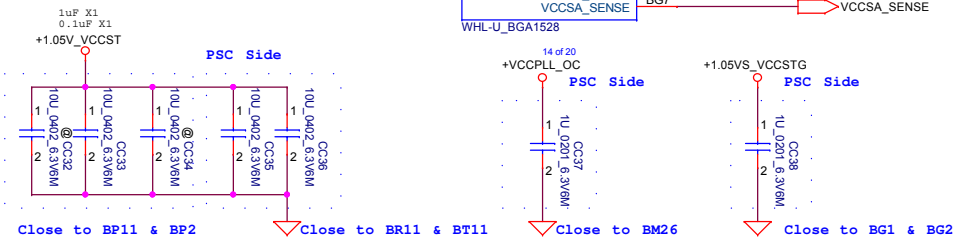
I(Max) : 0.2 A(+1.8VS)
RON(Max) : 25 mohm
V drop : 0.005 V

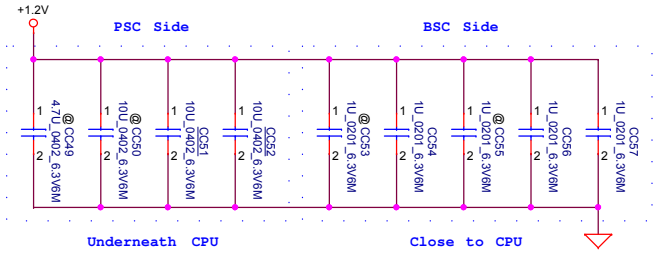
+1.05VALW TO +1.05VS_VCCIO











+1.2V TO +VCCPLL_OC

I(Max) : 120m A(+VCCPLL_OC)
RON(Max) : 6.2 mohm
V drop : 0.019 V

Security Classification	Compal Secret Data		
Issued Date	2018/09/21	Deciphered Date	2019/09/21

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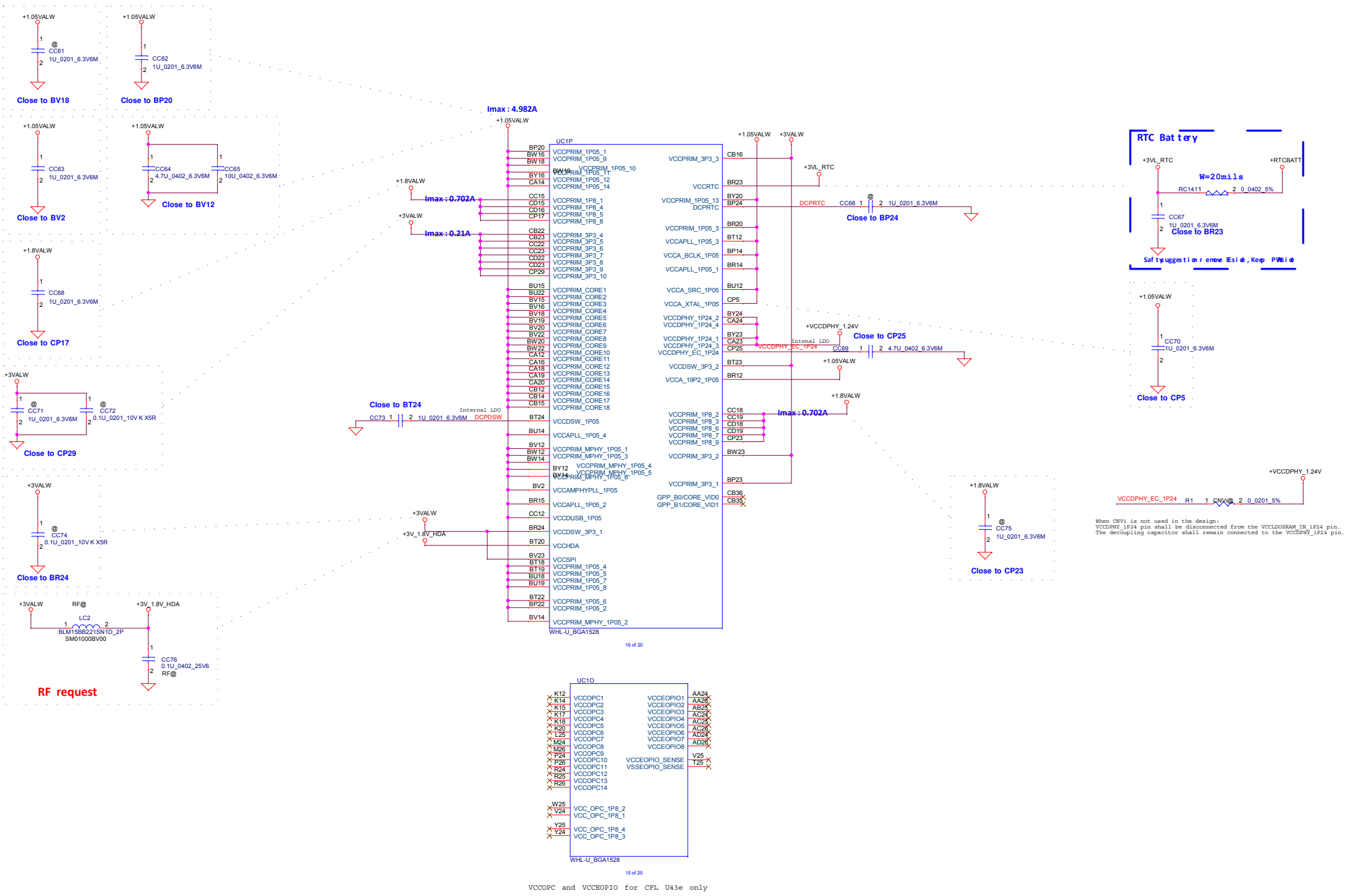
Compal Electronics, Inc.

Title: WHL-U(8/12)Power

Size	Document Number	Rev
Custom	LA-H101P	0.A

Date: Thursday, September 20, 2018 Sheet 13 of 51



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Issued Date	2018/09/21	Deciphered Date	2019/09/21

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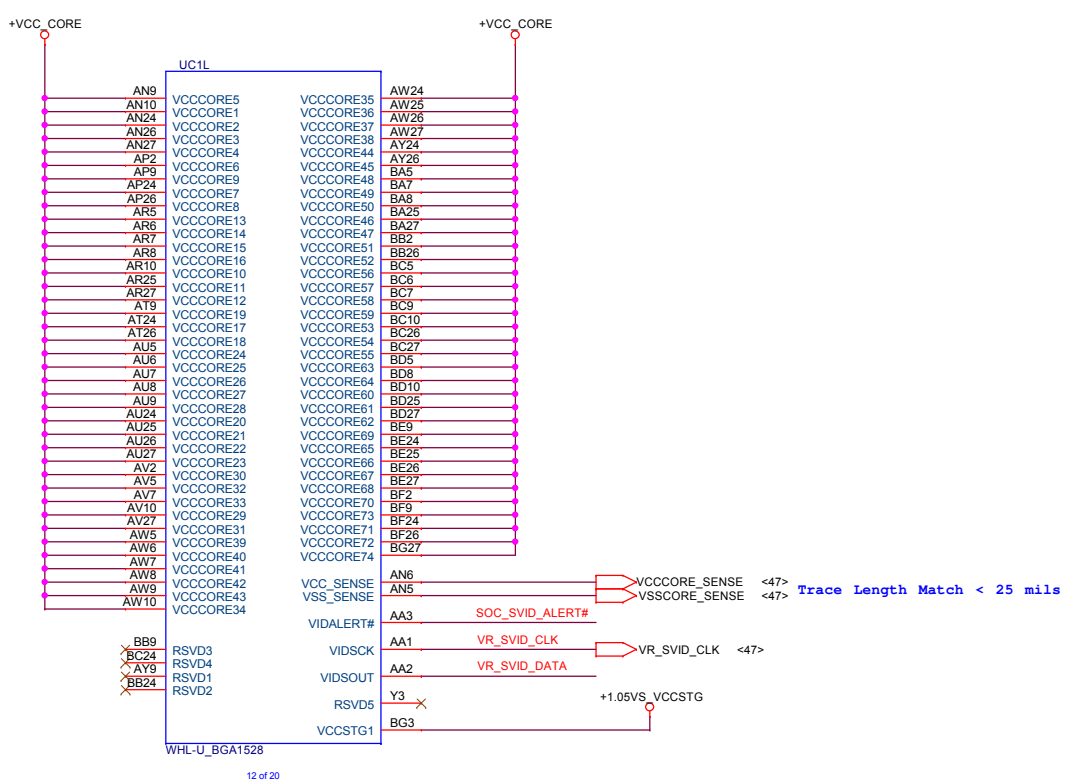
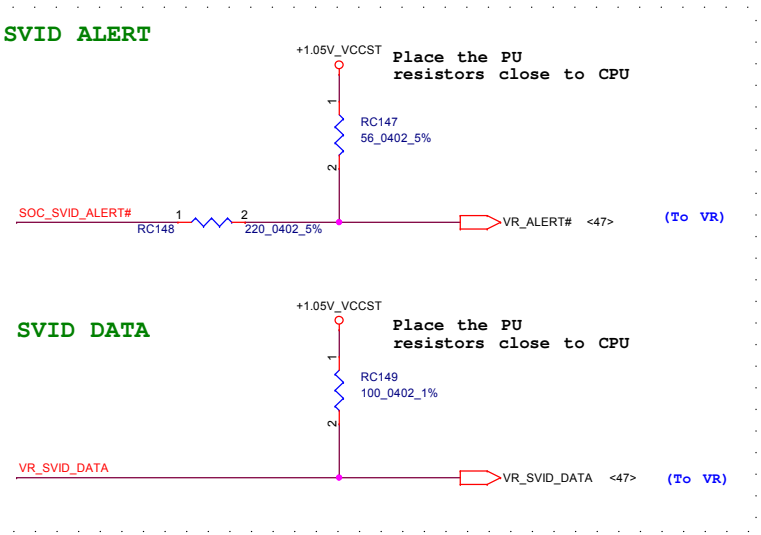
Compal Electronics, Inc.			
Title	WHL-U(9/12)Power		
Size: Custom	Document Number: LA-H101P		Rev: 0.A
Date: Thursday, September 20, 2018	Sheet 14 of 51		





Security Classification	Compal Secret Data		
Issued Date	2018/09/21	Deciphered Date	2019/09/21

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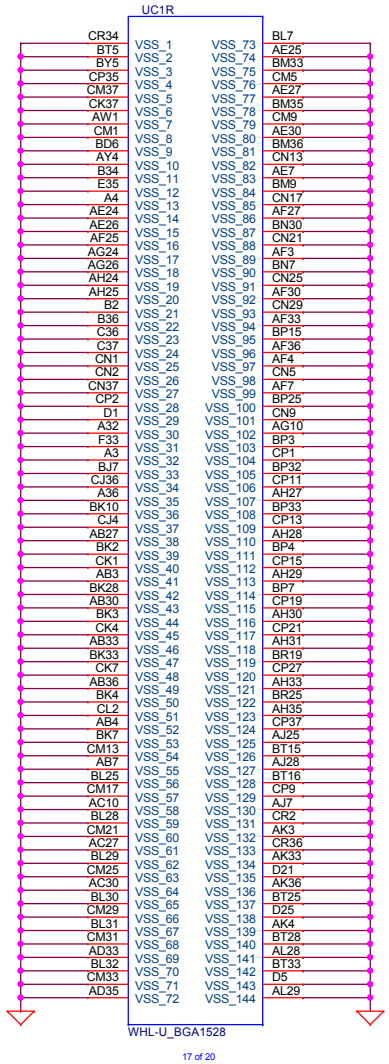
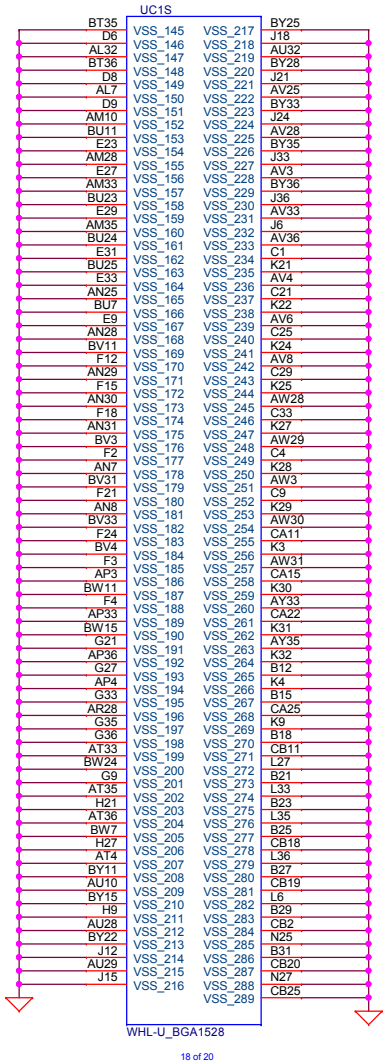
Compal Electronics, Inc.

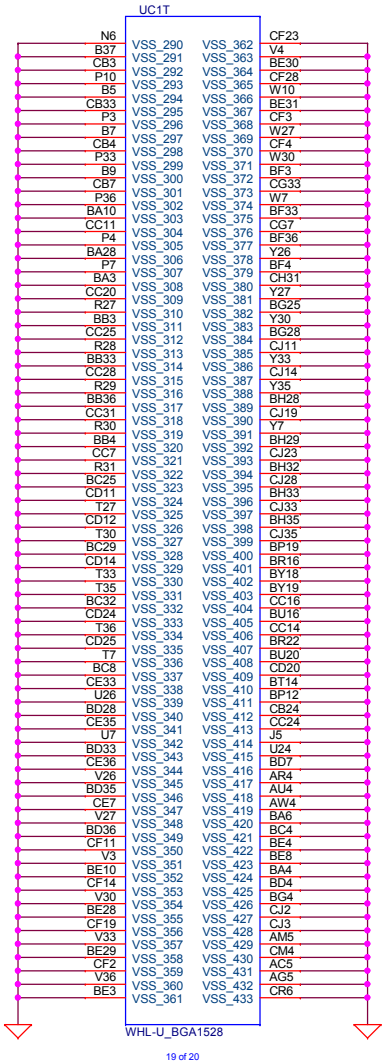
Title: WHL-U(10/12)Power,SVID

Size	Document Number	Rev
Custom	LA-H101P	0.A

Date: Thursday, September 20, 2018 Sheet 15 of 51







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Issued Date	2018/09/21	Deciphered Date	2019/09/21

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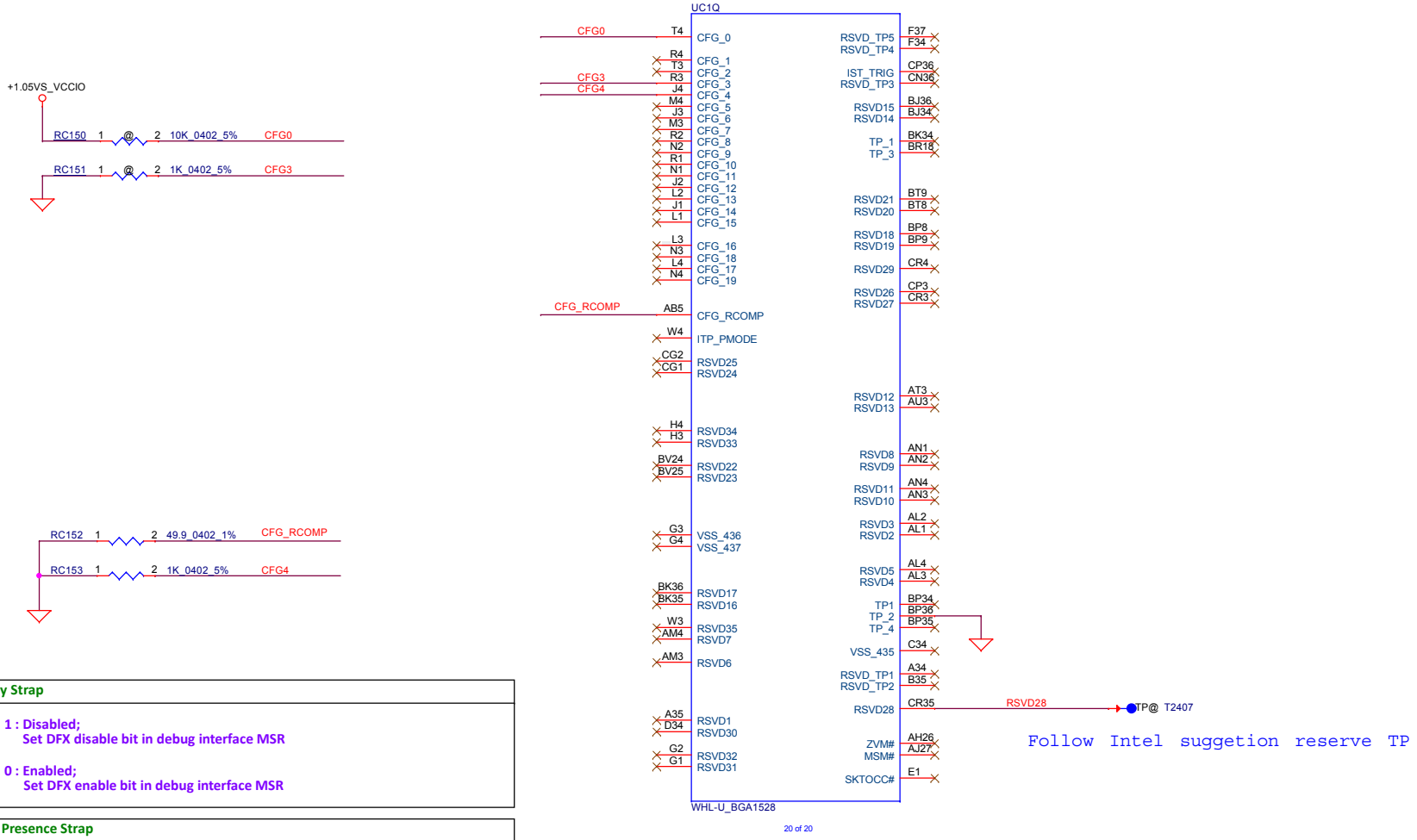
Compal Electronics, Inc.

Title: **WHL-U(11/12)GND**

Size	Document Number	Rev
Custom	LA-H101P	0.A

Date: Thursday, September 20, 2018 | Sheet 16 of 51



Follow Intel suggetion reserve TP

DFX Privacy Strap	
CFG3	1 : Disabled; Set DFX disable bit in debug interface MSR 0 : Enabled; Set DFX enable bit in debug interface MSR

Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port at t ached to E mbedded D sp ay port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

Security Classification	Compal Secret Data		
Issued Date	2018/09/21	Deciphered Date	2019/09/21

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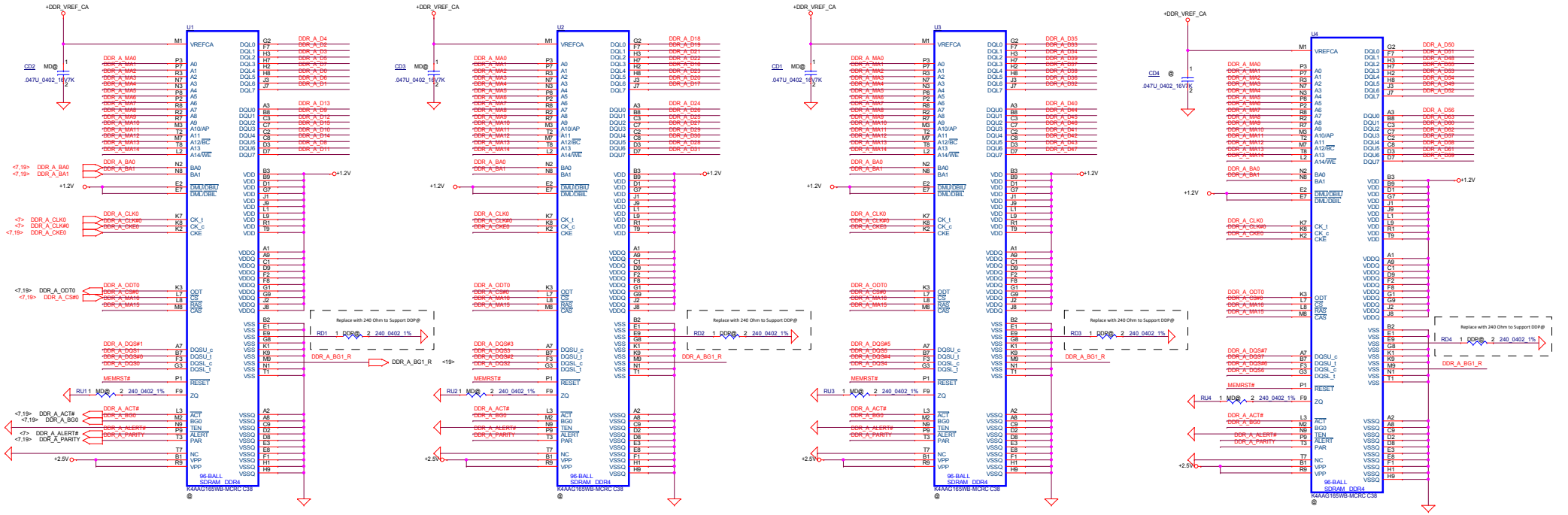
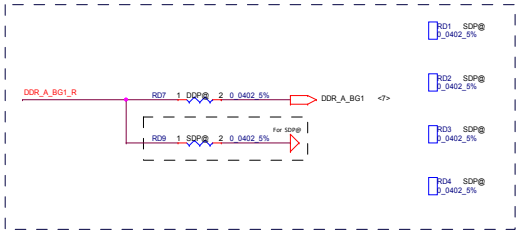
Compal Electronics, Inc.		
Title: WHL-U(12/12)CFG,RSVD		
Size: Custom	Document Number: LA-H101P	Rev: 0.A
Date: Thursday, September 20, 2018	Sheet 17 of 51	

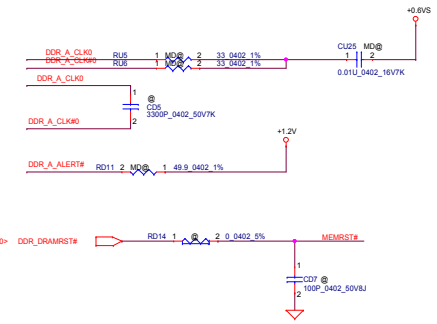
Interleaved Memory

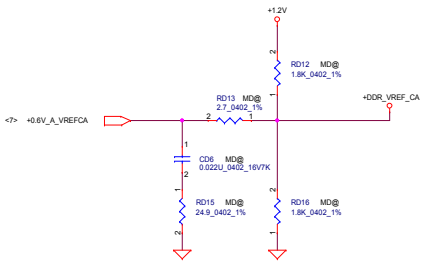


Co-lay for SDP / DDP Memory DIE



CLOCK TERMINATION





On Board RAM - Data Mapping

U4	DQ	U2	DQ	U3	DQ	U1	DQ
DQL0	D13	DQL0	D29	DQL0	D43	DQL0	D60
DQL1	D12	DQL1	D25	DQL1	D40	DQL1	D61
DQL2	D11	DQL2	D27	DQL2	D42	DQL2	D62
DQL3	D8	DQL3	D24	DQL3	D41	DQL3	D57
DQL4	D10	DQL4	D30	DQL4	D47	DQL4	D58
DQL5	D9	DQL5	D28	DQL5	D45	DQL5	D56
DQL6	D14	DQL6	D31	DQL6	D46	DQL6	D59
DQL7	D15	DQL7	D26	DQL7	D44	DQL7	D63
DQU0	D6	DQU0	D22	DQU0	D38	DQU0	D50
DQU1	D1	DQU1	D17	DQU1	D37	DQU1	D52
DQU2	D7	DQU2	D23	DQU2	D35	DQU2	D51
DQU3	D5	DQU3	D20	DQU3	D32	DQU3	D48
DQU4	D3	DQU4	D19	DQU4	D33	DQU4	D54
DQU5	D4	DQU5	D16	DQU5	D36	DQU5	D53
DQU6	D2	DQU6	D18	DQU6	D39	DQU6	D55
DQU7	D0	DQU7	D21	DQU7	D34	DQU7	D49

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Issued Date	2018/09/21	Deciphered Date	2019/09/21

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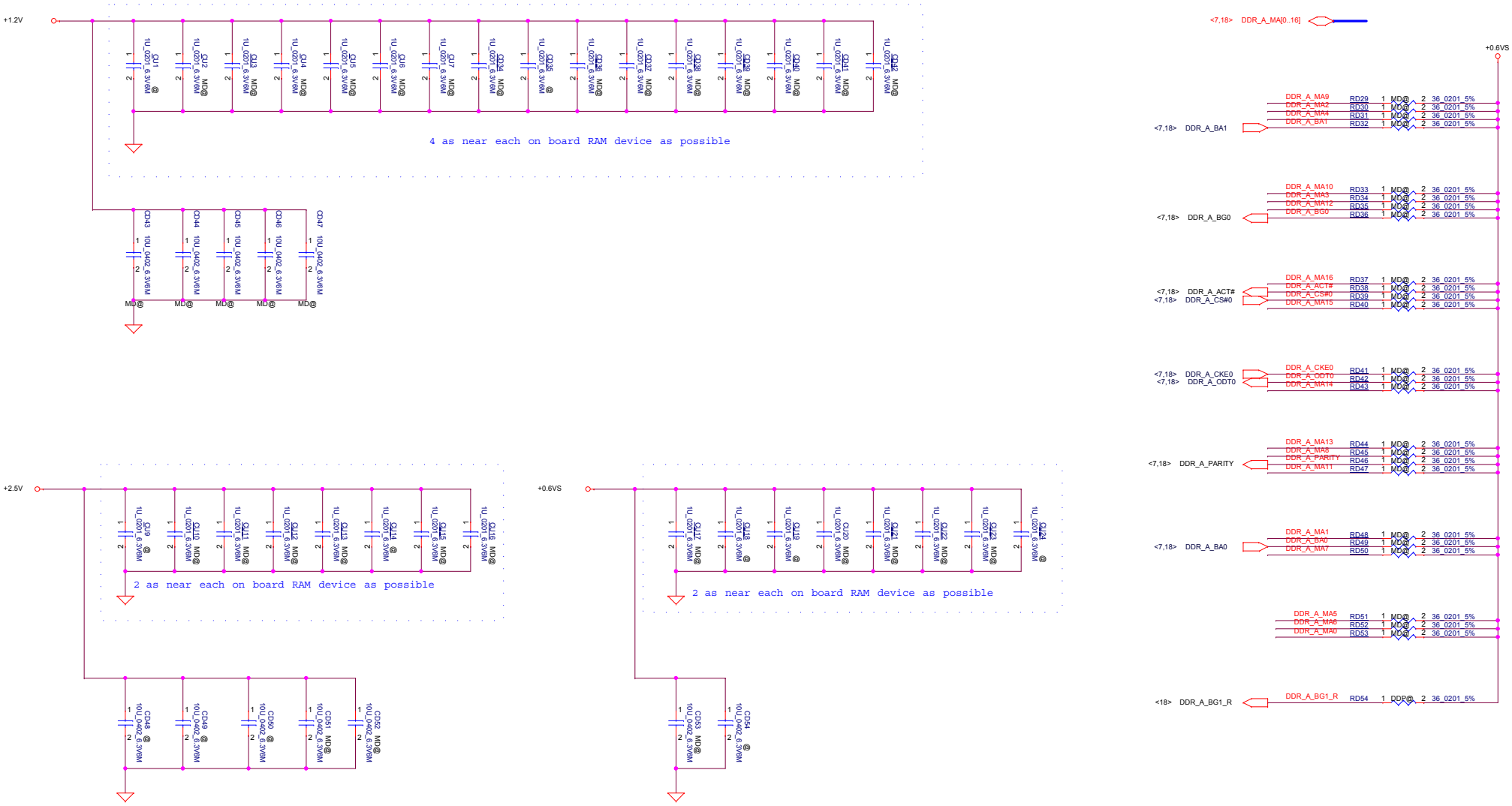
Title	DDR4 ON BOARD CHIPS		
Size	Document Number		Rev
Custom	LA-H101P		0.A
Date:	Thursday, September 20, 2018	Sheet	18 of 51



Security Classification	Compal Secret Data		
Issued Date	2018/09/21	Deciphered Date	2019/09/21

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Title	DDR4 MISC		
Size	Document Number		Rev
Custom	LA-H101P		0.A
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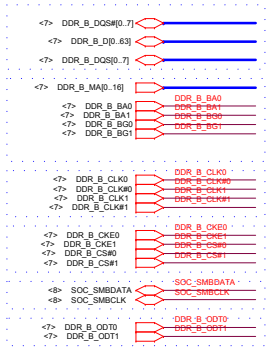
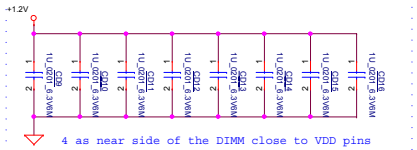
Standard Type

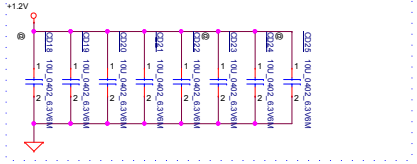
2-3A to 1 DIMMs/channel

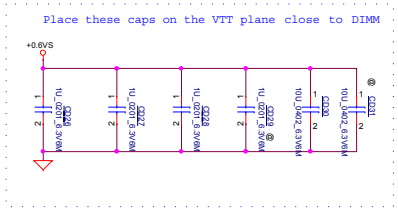


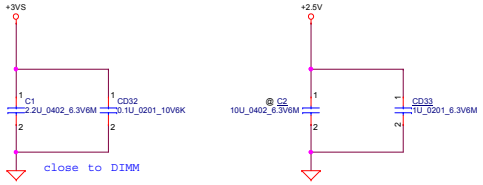
Layout Note:
Place near JDIMM1

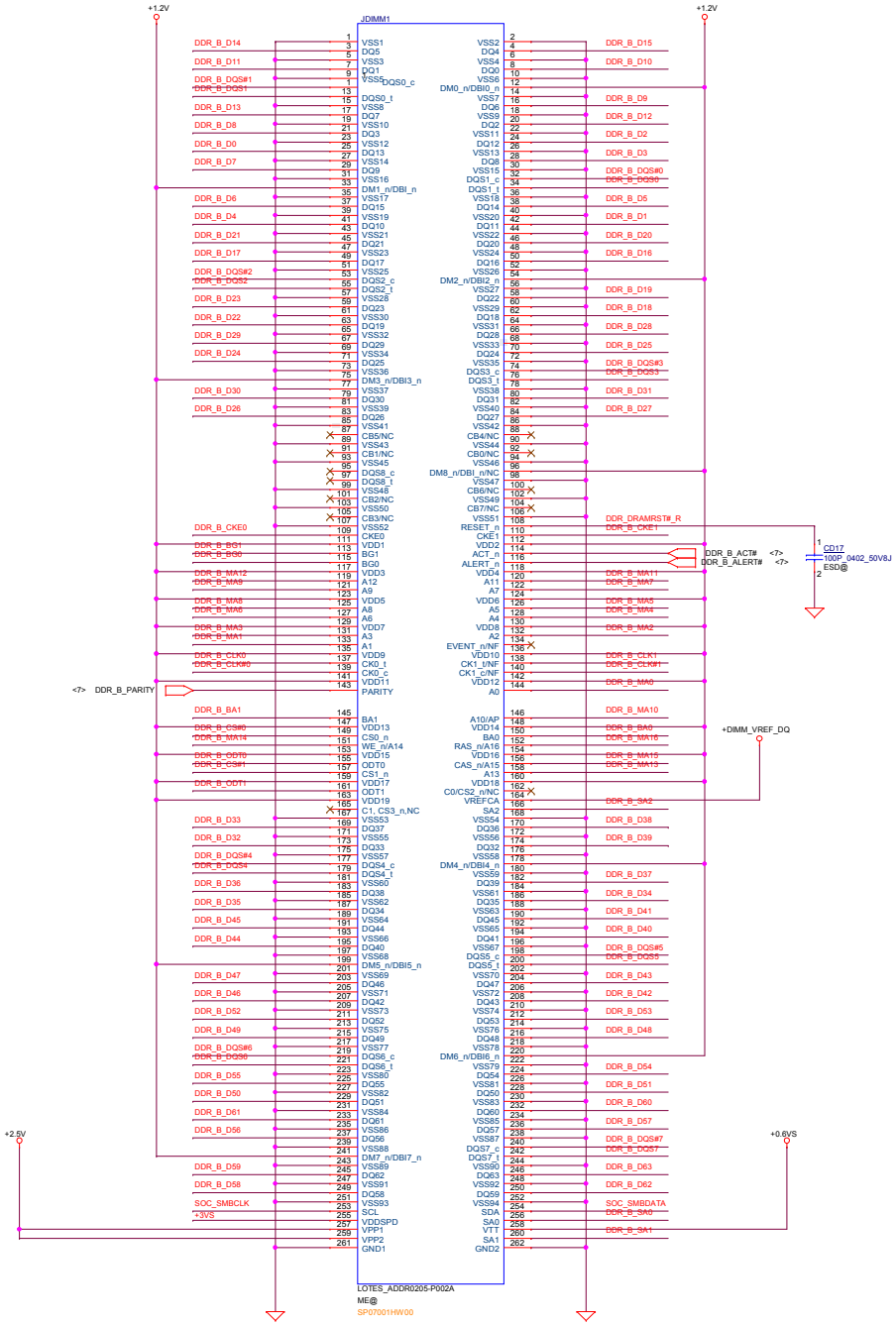
Note:
Check voltage tolerance of VREF_DQ at the DIMM socket

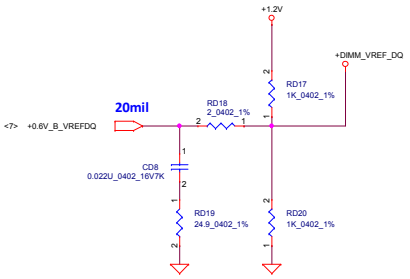


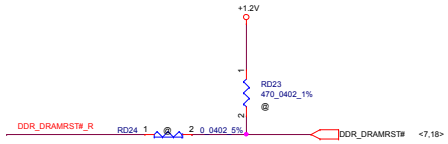




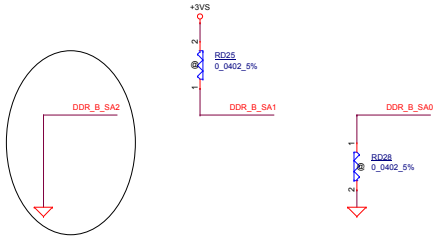








JDIMM1 ADDRESS (PLACE CLOSE TO DIMM)



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Issued Date	2018/09/21	Deciphered Date	2019/09/21

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Compal Electronics, Inc.

Title: **DDR4 DIMM**

Size: Custom | Document Number: **LA-H101P** | Rev: 0.A

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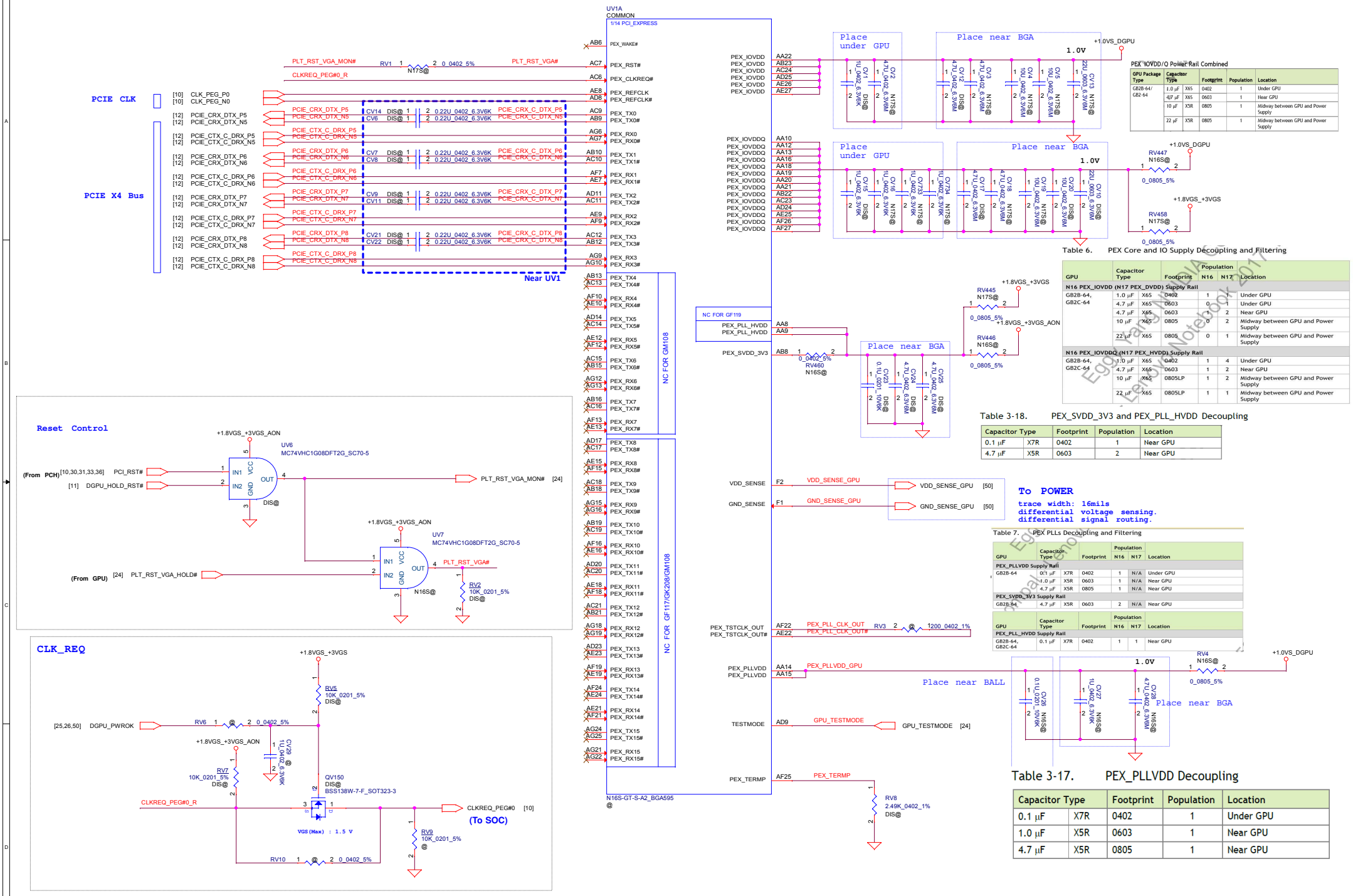

Security Classification	Compal Secret Data		
Issued Date	2017/10/27	Deciphered Date	2019/04/09

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Compal Electronics, Inc.

Title: NV(1/5)-PCIE

Size | Document Number: LA-H101P | Rev: 0.A

Date: Monday, October 22, 2018 | Sheet 21 of 53

IFPA/B

UV1G
COMMON
4/14 IFPAB

IFPAB_RSET AA6
IFPAB_PLLVDD V7
IFPAB_PLLVDD W7
IFPA_IOVDD W8
IFPB_IOVDD Y8

NC FOR GF117/GM108

IFPA_TXC# AC4
IFPA_TXC AC3
IFPA_TXD0# Y3
IFPA_TXD0 Y4
IFPA_TXD1# AA2
IFPA_TXD1 AA3
IFPA_TXD2# AA1
IFPA_TXD2 AB1
IFPA_TXD3# AA5
IFPA_TXD3 AA4
IFPB_TXC# AB4
IFPB_TXC AB5
IFPB_TXD4# AB2
IFPB_TXD4 AB3
IFPB_TXD5# AD2
IFPB_TXD5 AD3
IFPB_TXD6# AD1
IFPB_TXD6 AE1
IFPB_TXD7# AD5
IFPB_TXD7 AD4

NC FOR GF117/GM108

GF117 | NC | GPIO14 B3

IFPAB
N16S-GT-S-A2_BGA595
@

DAC_A

UV1K
COMMON
3/14 DACA

GF117/GM108		GF117	GM108/GK208	
DACA_VDD W5	NC	NC	I2CA_SCL	B7
DACA_VREF AE2	TSEN_VREF	NC	I2CA_SDA	A7
DACA_RSET AF2	NC	NC	DACA_HSYNC	AE3
		NC	DACA_VSYNC	AE4
		NC	DACA_RED	AG3
		NC	DACA_GREEN	AF4
		NC	DACA_BLUE	AF3
		GM108 GF117	GK208	

N16S-GT-S-A2_BGA595
@

Note:
IFPC/D/E/F interface are XVDDs pin for N17S GPU, and connect them to NVVDD power for improving NVVDD power rail routing

Table 8. Other PLLs Power Decoupling and Filtering

GPU	Type	Footprint	Population N16	N17	Location
PLLVDD (N17: XS_PLLVDD) Supply Rail					
GB2B-64, GB2C-64	0.1 µF X7R	0402	1	1	Under GPU
	22 µF X5R	0805	1	0	Near GPU
	Bead Type				
	L2=30 Ω (ESR=0.05 Ω)	0402	1	0	Near GPU
SP_PLLVDD and VID_PLLVDD Combined Supply Rails					
GB2B-64, GB2C-64	0.1 µF X7R	0402	2	2	Under GPU
	10 µF X5R	0603	1	0	Near GPU
	47 µF X5R	0805	1	0	Near GPU
	Bead Type				
	L2=300 Ω (ESR=0.2 Ω)	0603	1	0	Near GPU

IFPC

UV1H
COMMON
5/14 IFPC

IFPC_RSET T6
IFPC_PLLVDD M7
IFPC_PLLVDD N7
IFPC_IOVDD P6

NC FOR GF117/GM108

IFPC

GF119/GK208
DVI/HDMI DP
I2CW_SDA I2CW_SCL IFPC_AUX# N5 IFPC_AUX N4
TXC TXC IFPC_L3# N3 IFPC_L3 N2
TXD0 TXD0 IFPC_L2# R3 IFPC_L2 R2
TXD1 TXD1 IFPC_L1# R1 IFPC_L1 T1
TXD2 TXD2 IFPC_L0# T3 IFPC_L0 T2

NC FOR GF117/GM108

GF117 | NC | GPIO15 C3

N16S-GT-S-A2_BGA595
@

IFPD

UV1I
COMMON
6/14 IFPD

IFPD_RSET U6
IFPD_PLLVDD T7
IFPD_PLLVDD R7
IFPD_IOVDD R6

NC FOR GF117/GM108

IFPD

GF119/GK208
DVI/HDMI DP
I2CX_SDA I2CX_SCL IFPD_AUX# P4 IFPD_AUX P3
TXC TXC IFPD_L3# R5 IFPD_L3 R4
TXD0 TXD0 IFPD_L2# T5 IFPD_L2 T4
TXD1 TXD1 IFPD_L1# U4 IFPD_L1 U3
TXD2 TXD2 IFPD_L0# V4 IFPD_L0 V3

NC FOR GF117/GM108

GF117 | NC | GPIO17 D4

N16S-GT-S-A2_BGA595
@

IFPE/F

UV1J
COMMON
7/14 IFPEF

IFPEF_PLLVDD J7
IFPEF_PLLVDD K7
IFPEF_RSET K6

IFPE

IFPE_IOVDD H6
IFPF_IOVDD J6

NC FOR GF117/GM108
NC FOR GF117/GK208/GM108

GF119/GK208
DVI-DL DVI-SL/HDMI DP
I2CY_SDA I2CY_SCL IFPE_AUX# J3 IFPE_AUX J2
TXC TXC IFPE_L3# J1 IFPE_L3 K1
TXD0 TXD0 IFPE_L2# K3 IFPE_L2 K2
TXD1 TXD1 IFPE_L1# M3 IFPE_L1 M2
TXD2 TXD2 IFPE_L0# M1 IFPE_L0 N1
NC FOR GK208

HPD_E HPD_E GPIO18 C2
NC FOR GF117

GF119/GK208
DVI-DL DVI-SL/HDMI DP
I2CZ_SDA I2CZ_SCL IFPF_AUX# H4 IFPF_AUX H3
TXC TXC IFPF_L3# J5 IFPF_L3 J4
TXD3 TXD3 TXD0 TXD0 IFPF_L2# K5 IFPF_L2 K4
TXD4 TXD4 TXD1 TXD1 IFPF_L1# L4 IFPF_L1 L3
TXD5 TXD5 TXD2 TXD2 IFPF_L0# M5 IFPF_L0 M4
NC FOR GK208

HPD_F GPIO19 F7
NC FOR GF117

IFPF

N16S-GT-S-A2_BGA595
@

+1.8VGS_+3VGS
RV448 N17S@ 0_0805_5%
+1.0VS_DGPU
LV1 N16S@ HCB1005KF-300T25_2P
GPU_PLLVDD
Place near balls
CV30 22U_0603_6.3V6M N16S@
CV31 0.1U_0201_10V K X5R DIS@

GPU Package	PLL Rail	Capacitor Type		Footprint	Population	Location
GB2-64, GB2B-64, GB4B-128	PLLVDD	0.1 µF	X7R	0402	1	Under GPU
		22 µF	X5R	0805	1	Near GPU
		Bead Type				
		30 Ω (ESR=0.05 Ω)		0402	1	Near GPU

PLLVDD
RV457 N17S@ 0_0805_5%
+1.0VS_DGPU
RV456 N16S@ 0_0805_5%
Place near BGA
Place near balls
VID_PLLVDD
CV32 22U_0603_6.3V6M N16S@
CV33 22U_0603_6.3V6M N16S@
CV34 10U_0402_6.3V6M N16S@
CV35 0.1U_0201_10V K X5R DIS@
CV36 0.1U_0201_10V K X5R DIS@

Table 3-33. SP_PLLVDD Power Rail Filtering [1]

GPU Package	PLL Rails	Capacitor Type		Footprint	Population	Location
GB2-64 GB2B-64 GB4B-128 GB3B-256	SP_PLLVDD (+ VID_PLLVDD)[1]	0.1 µF	X7R	0402	1 per ball	Under GPU
		10 µF	X5R	0603	1	Near GPU
		47 µF	X5R	0805	1	Near GPU
		Bead Type				
		300 Ω (ESR=0.2 Ω)		0603	1	Near GPU

Note:
1. SP_PLLVDD and VID_PLLVDD power rails can be combined for customers who either do not use VGA display or uses VGA display with maximum resolution lower than 1024 x 768 with a 240 Hz refresh rate.

X'TAL

UV1M
COMMON
9/14 XTAL_PLL

PLLVDD L6
SP_PLLVDD M6
VID_PLLVDD N6
XTALSSIN A10
XTALIN C11

VID_PLLVDD	NC
GF119/GK208	GF117/GM108

XTALOUTBUFF C10
XTALOUT B10

N16S-GT-S-A2_BGA595
@

90-OHM DIFF Impedance for XTALIN & XTALOUT.

RV12 DIS@ 10K_0402_1%
RV11 @ 10K_0402_1% +1.8VGS_+3VGS_AON
RV13 DIS@ 10K_0402_1%
XTAL_OUTBUFF
RV14 DIS@ 1.5K_0402_1%
YV1 27MHZ_10PF_XRCGB27M000F2P18R0 SJ10000UJ00
NC NC DIS@
CV37 DIS@ 18P_0402_50V8J
CV38 DIS@ 18P_0402_50V8J

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GPU_Decoupling CAPs @ Power Page

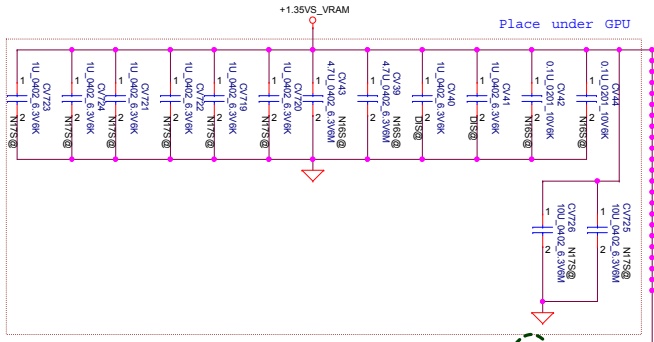
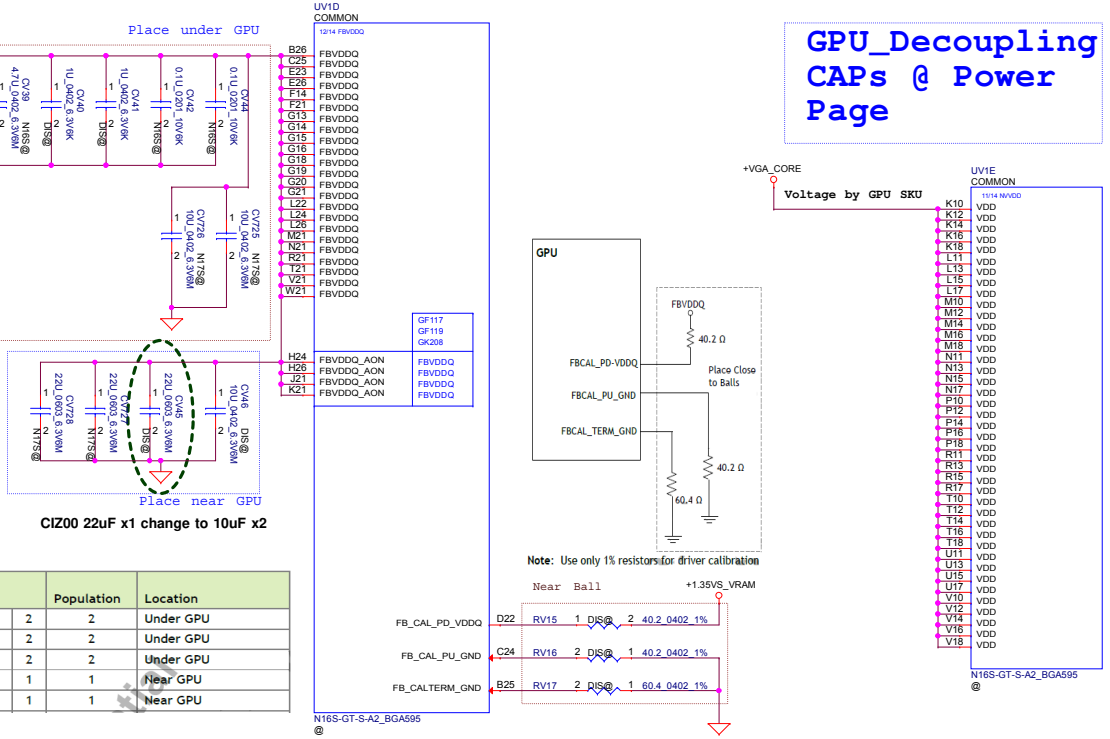
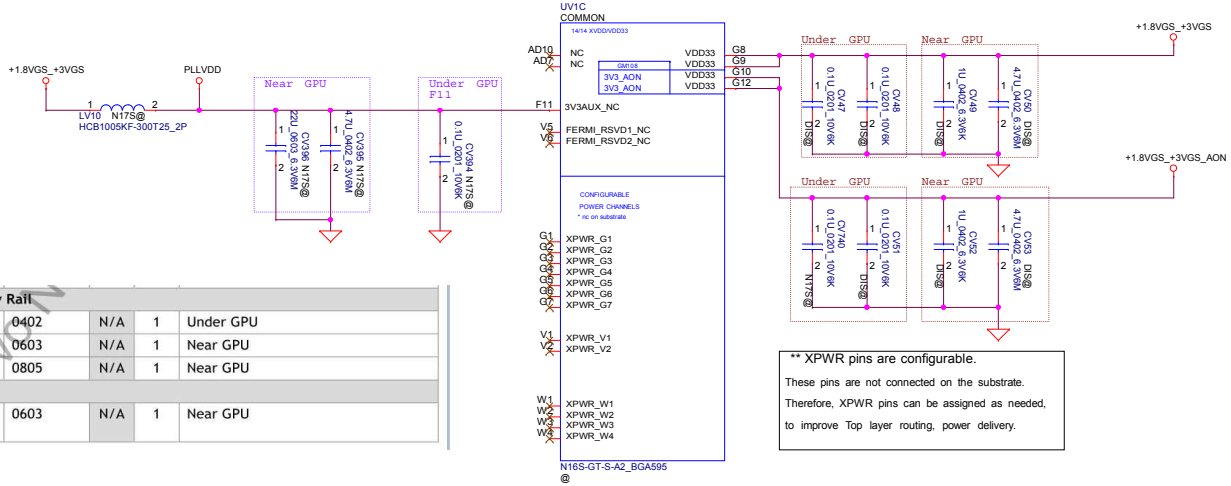


Table 4. Frame Buffer Core and IO Decoupling and Filtering

GPU	Capacitor Type	Footprint	Population N16	Population N17	Location
FBVDD/Q Supply Rail for GDDR5					
GB2B-64, GB2C-64	0.1 µF	X7R 0402	2	0	Under GPU
	1 µF	X7R 0603	2	8	Under GPU
	4.7 µF	X6S 0603	2	0	Under GPU
	10 µF	X6S 0603	0	2	Under GPU
	10 µF	X6S 0603	1	1	Near GPU
	22 µF	X6S 0603W	1	3	Near GPU



GPU Package Type	Capacitor Type	Footprint		Population	Location
GB2B-64/ GB2-64 GDDR5	0.1 µF	X7R	0402	2	Under GPU
	1 µF	X7R	0603	2	Under GPU
	4.7 µF	X6S	0603	2	Under GPU
	10 µF	X5R	0805	1	Near GPU
	22 µF	X5R	0805	1	Near GPU



NC (N17: GPCPLL_AVDD) Supply Rail						
GB2C-64	0.1 µF	X7R	0402	N/A	1	Under GPU
	4.7 µF	X6S	0603	N/A	1	Near GPU
	22 µF	X6S	0805	N/A	1	Near GPU
	Bead Type					
	L=30 Ω (ESR=0.010 Ω)		0603	N/A	1	Near GPU

GPU Package	Rail	Capacitor Type		Footprint		Population	Location
GB2-64 GB2B-64 GB4B-128 GB3B-256	3V3_MAIN	0.1µF	X6S	0402	1	2	Under GPU
		1 µF	X5R	0603	1	1	Near GPU
		4.7 µF	X5R	0603	1	1	Near GPU
GB2-64 GB2B-64 GB4B-128 GB3B-256	3V3_AON	0.1µF	X6S	0402	1	1	Under GPU
		1 µF	X5R	0603	1	1	Near GPU
		4.7 µF	X5R	0603	1	1	Near GPU

Note: This table is for non-SLI mode. For SLI mode, please refer to the MIO Decoupling table.

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GPIO

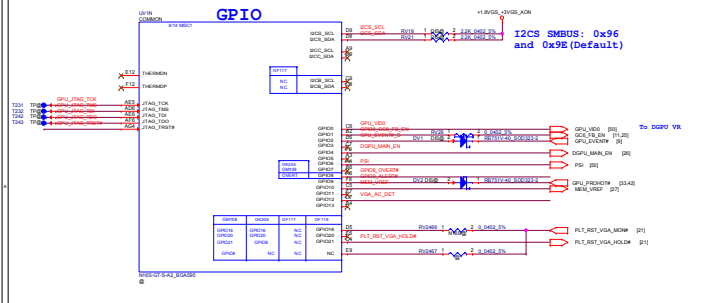
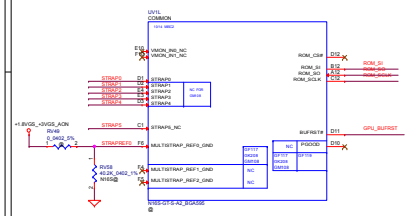


Table 12-2. GB2B-64 and GB4B-128 GPIO Description

GPIO Number	GPIO Name	I/O	Functional Description	NO Termination
GPIO0	GCA_FB_EN	O	FB Enable for GC6 2.0, Open Source	10 kΩ pull-down
GPIO1	MEM_VID_CTL	O	Memory voltage control	Pull-up/pull-down to set the FBVDDQ Boot voltage
GPIO2	LCD_BL_PWM	O	Panel Backlight PWM Brightness Control	100 kΩ pull-down
GPIO3	LCD_VCC	O	Panel Power Enable	100 kΩ pull-down
GPIO4	LCD_BLEN	O	Panel Backlight Enable	100 kΩ pull-down
GPIO5	3V3_MAIN_EN	O	GPU power sequencing for GC6 2.0, Open Drain	10 kΩ pull-up to 3V3_AON
GPIO6	GPU_EVENT#	I	GPU wake signal for GC6 2.0	10 kΩ pull-up to 3V3_AON
GPIO7	3DVision	O	3D Vision L/R signal	100 kΩ pull-down
GPIO8	SYS_PEX_RST_MON#	I	System side PERstn# monitor	10 kΩ pull-up to 3V3_AON unless actively driven
GPIO9	THERM_ALERT	I/O	Active low Thermal Alert, Open Drain	10 kΩ pull-up to 3V3_AON
GPIO10	MDA_VREF_CTL	O	Memory VREF Control	100 kΩ pull-down
GPIO11	PWM_VID	O	GPU Core VDD PWM control signal	
GPIO12	PWR_LEVEL	I	AC power detect or power supply throttle input	100 kΩ pull-up to 3V3_AON
GPIO13	PSI	O	Phase Shedding	10K pull-up to 3V3_AON to enable two phase.
GPIO14	HPD_A	I	Hot Plug Detect for IFPA used as DisplayPort for IFPAB when used as Dual Link DVI	See Figure 12-1
GPIO15	HPD_C	I	Hot Plug Detect for IFPC	See Figure 12-1
GPIO16	FRAME_LOCK#	I	Active Low Frame Lock, Open Drain	10 kΩ pull-up to 3V3_AON; Not available for GB2B-64
GPIO17	HPD_D	I	Hot Plug Detect for IFPD	See Figure 12-1
GPIO18	HPD_E	I	Hot Plug Detect for IFPE	See Figure 12-1
GPIO19	HPD_F or HPD_B	I	Hot Plug Detect for IFPF or for IFPB when used as DisplayPort	See Figure 12-1
GPIO20	Reserved			
GPIO21	GPU_PEX_RST_MON#	O	GPU PCIe self-reset control, Open Drain	10 kΩ pull-up to 3V3_AON
OVERT	OVERT	I/O	Catastrophic Over Temperature	100 kΩ pull-up to 3V3_AON



10.2.1 Unconnected Signals (NC)

Do not route unused I²C signals on the PCB in order to protect the GPU from outside ESD risk. If unused traces are routed, the signals should be pulled down to ground with 1.8 kΩ resistors.

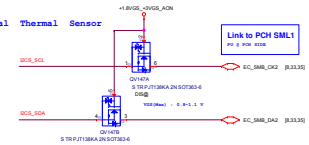
10.2.2 I²CS Slave Address

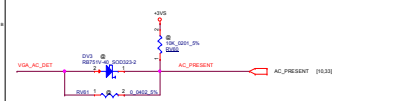
N16x GPUs use I²CS slave address 0x96h for NVIDIA internal testing. I²C address 0x96h must not be used by other I²C devices on the same bus as the GPU to avoid address conflict. The SMB_ALT_ADDR strap does not affect this 0x96h address. Refer to Chapter 15 (Straps) for a list of useful I²CS Slave addresses can be used with SMB_ALT_ADDR strapping.

16.3.3 Internal Thermal Sensor Interface

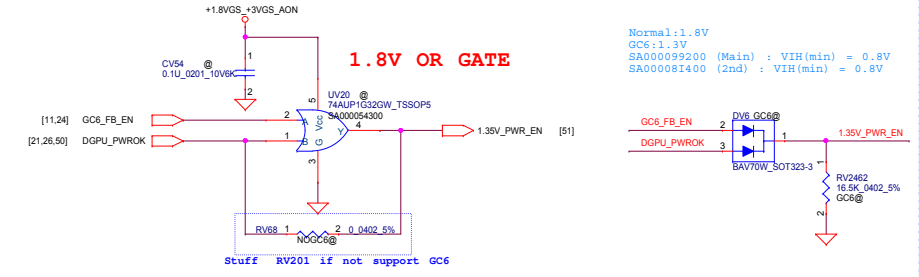
The internal thermal sensor can be accessed through the I²CS interface as described in the I²C chapter. This interface is compliant with the System Management Bus (SMBus) Specification (Version 2.0). The interface supports PEC and SMBus Timeout as well as Read Byte and Read Byte with PEC. Writes to the internal thermal sensor registers through the I²CS interface by the system is not supported. The default port address to access the internal thermal sensor over the I²CS is 0x9E. Table 16-1 describes the byte-wise registers accessible through the I²CS interface.

Internal Thermal Sensor





For GC6



From DG-07158-001_v05_secured(NVDIA Spec)

7.1.8 CKE* Signal

Two copies of the clock enable signal (CKE*) are provided for each memory partition of the GPU (Figure 7-4). These are connected to two DRAM components in the standard mode as point-to-point connections. The two signals are shared in the clamshell mode that will have four DRAM components (Figure 7-5). The CKE* signal requires a 10 kΩ pull-up resistor. This pull-up placement is not critical. The ODT is not provided for these signals.

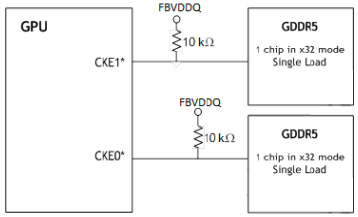


Figure 7-4. Clock Enable (CKE*) Signal Connection, ×32 Mode

7.1.7.3 RST* Signal

Each channel (32-bit interface) of the GPU provides a single reset signal (Figure 7-3). This is connected to one DRAM component in the standard mode and two DRAM components in the clamshell mode. This signal requires one 10 k Ω pull-down resistor in standard mode or in clamshell mode. The placement of this pull-down resistor should be at the end of the daisy-chain of this trace. The ODT is not provided for this signal.

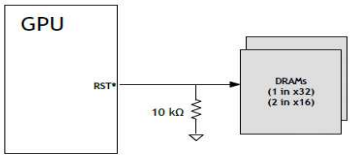


Figure 7-3. Reset Signal Connection

GPU Package	Rail	Capacitor Type		Footprint	Population	Location
GB2-64/ GB2B-64	FBx_PLL_AVDD and FB_DLL_AVDD Combined	0.1 µF	X7R	0402	2	Under GPU
		22 µF	X5R	0805	1	Near GPU
		Bead Type				
		30 Ω (ESR=0.010 Ω)		0603	1	Near GPU

Table 5. Frame Buffer PLLs Decoupling and Filtering

GPU	Capacitor Type		Footprint	Population N16	Population N17	Location
FB PLL Supply Rail for GDDR5						
GB2B-64, GB2C-64	0.1 µF	X7R	0402	2	4	Under GPU
	22 µF	X6S	0805	1	1	Near GPU
	Bead Type					
	30 Ω (ESR=0.010 Ω)		0603	1	1	Near GPU

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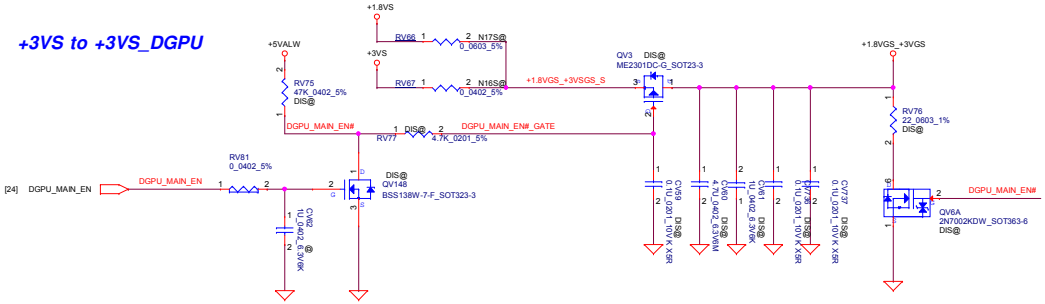
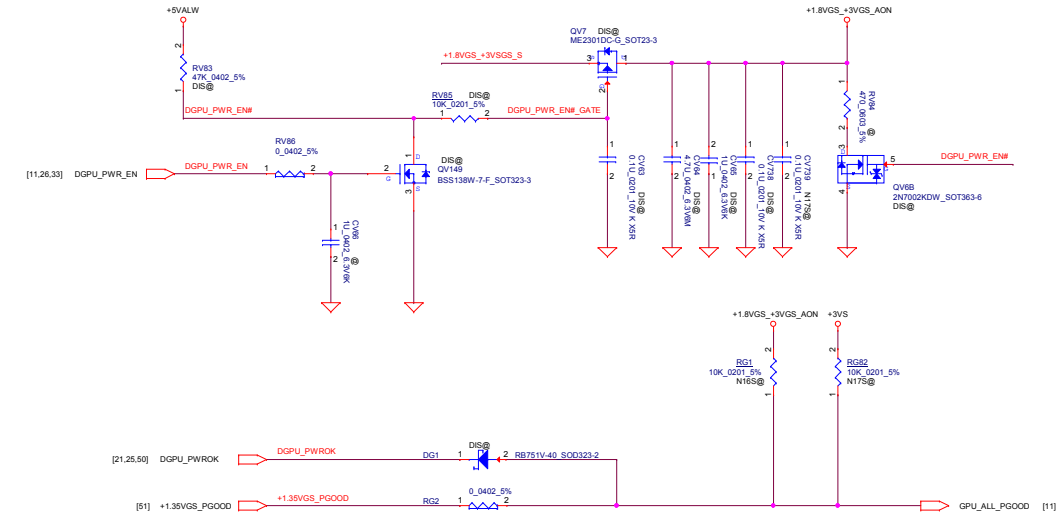
+3VS to +3VS_DGPU



+3VS to +3VS_DGPU_AON



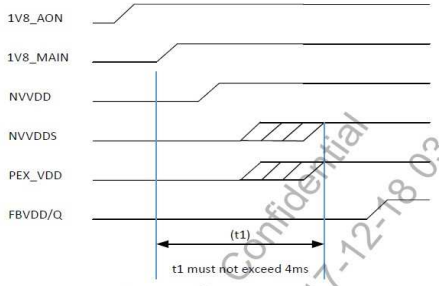
7.3.2.1 Power-Up Sequence

The following power-up sequence is required:

1V8_AON ➔ 1V8_MAIN ➔ NVVDD ➔ NVVDDS / PEX_DVDD ➔ FBVDD(Q)

- All GPU power rails must ramp up after 1V8_AON.
- FBVDD(Q) should ramp up after NVVDDS and PEX_DVDD.

All other 1.8V power rails can ramp up with 1V8_MAIN including PEX_HVDD and all PLLVDD rails; all other 1V power rails can ramp up with PEX_DVDD.



re 7.5 Example of Power-Up Sequencing Order

7.3.2.2 Power-Down Sequence

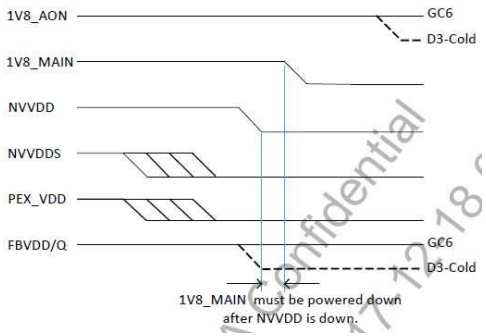
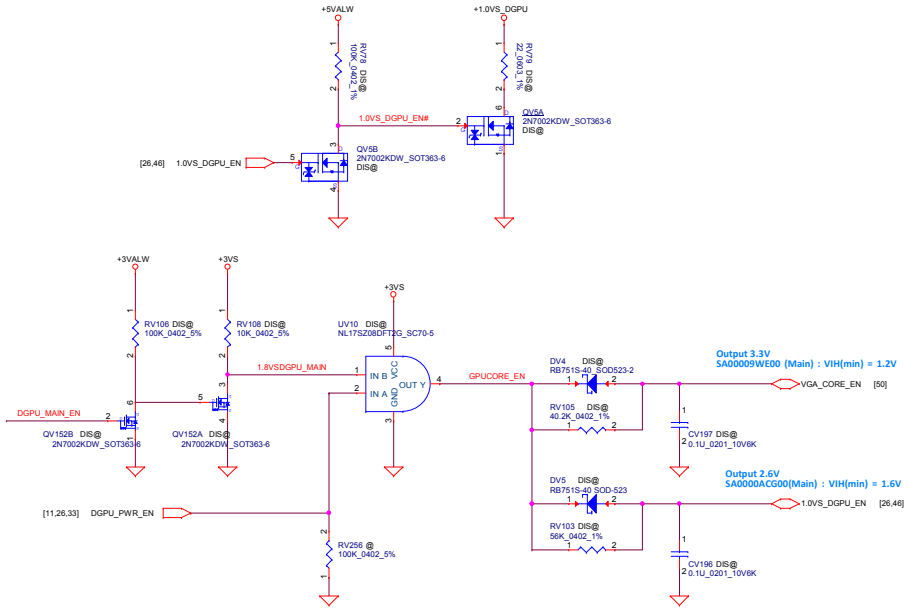


Table 7. Output EDP-Continuous

Product	NVVDD — (A)	GPU FBIO 1.35V[4] (A)	FB Total[5] 1.35V[4] (A)	1.0V Total[1] 1.0V[4] (A)	1.8V Total[2] 1.8V[4] (A)
N17S-LG	15.4	2.5	5.0	0.1	0.2
N17S-G1	30.0	3.0	5.6	0.1	0.3
N17S-G0[6]	27.8	3.2	5.8	0.2	0.5
N17S-G2[6]	28.6	3.2	5.8	0.2	0.5



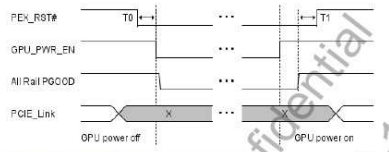


Figure 8.9 GC OFF Entry/Exit Timing Diagram

Table 8.1 GC OFF Timing Parameters

Symbol	Description	Min	Max	Units
T0	PEX_RST# assertion to GPU_PWR_EN=0	>0	5	ms
T1	All GPU power rail up and stable to PEX_RST# de-assertion	0.1	5	ms

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Title	DGPU_DC/DC Interface		
Size	Document Number LA-H101P		Rev 0.A
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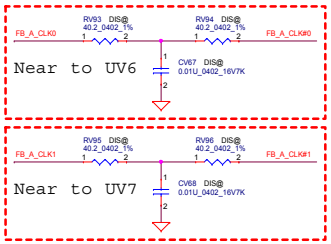
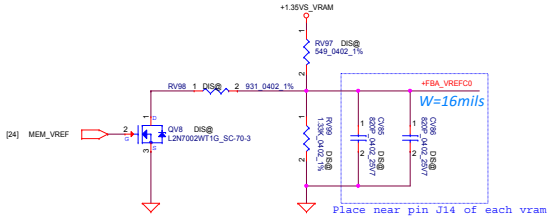
VRAM Memory Partition A

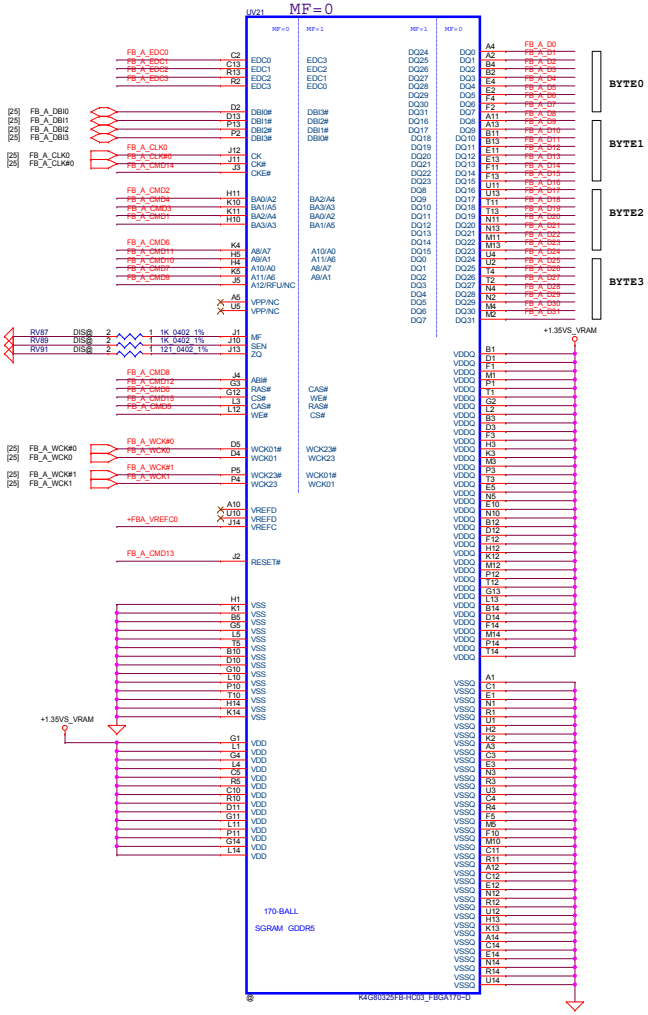
Table 7-4. GDDR5 Mode H Mapping

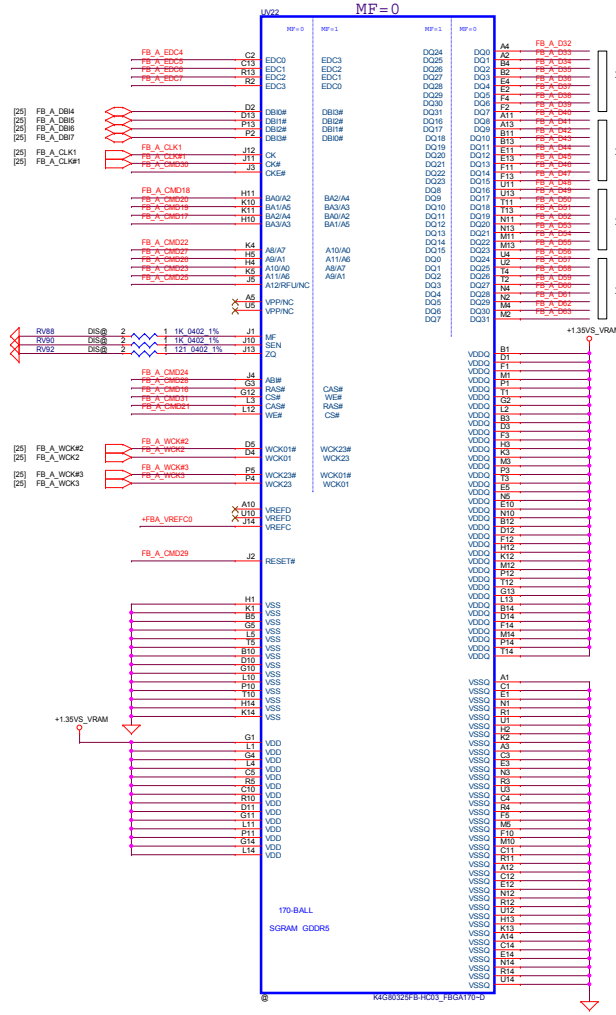
GB2-64, GB2B-64, GB4B-128	Channel 0 0..31	GB2-64, GB2B-64, GB4B-128	Channel 1 32..63
CMD0	CS*	CMD16	CS*
CMD1	A3_BA3	CMD17	A3_BA3
CMD2	A2_BA0	CMD18	A2_BA0
CMD3	A4_BA2	CMD19	A4_BA2
CMD4	A5_BA1	CMD20	A5_BA1
CMD5	WE*	CMD21	WE*
CMD6	A7_A8	CMD22	A7_A8
CMD7	A6_A11	CMD23	A6_A11
CMD8	ABI*	CMD24	ABI*
CMD9	A12_RFU	CMD25	A12_RFU
CMD10	A0_A10	CMD26	A0_A10
CMD11	A1_A9	CMD27	A1_A9
CMD12	RAS*	CMD28	RAS*
CMD13	RST*	CMD29	RST*
CMD14	CKE*	CMD30	CKE*
CMD15	CAS*	CMD31	CAS*
GB2-64, GB2B-64, GB4B-128	Channel 0 & 1		
CMD32	Not used		
CMD33[1]	Not used		
CMD34	DEBUG0[2]		
CMD35	DEBUG1[2]		

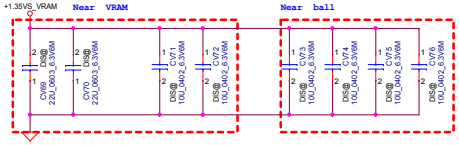
Notes:
1. Not available in GB2-64 and GB2B-64 packages.
2. GPU debug pins not connected to VRAM, see section 7.1.13.

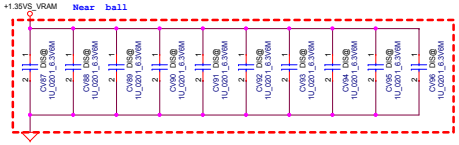


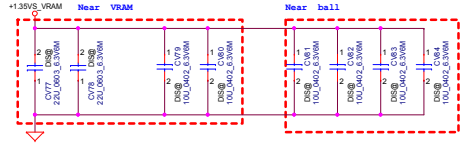


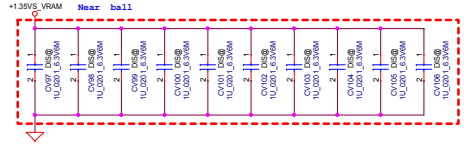












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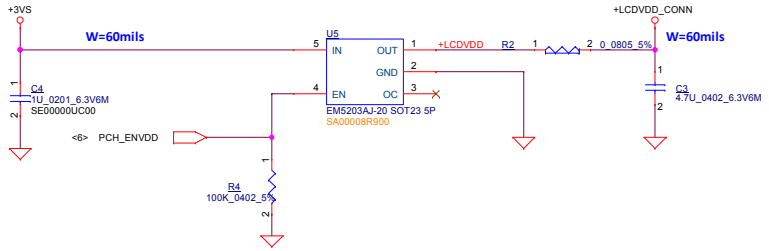
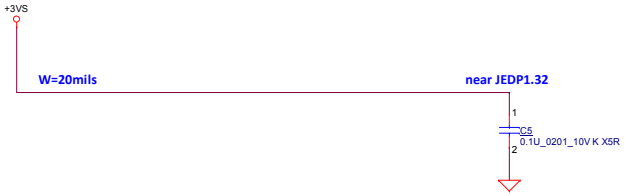
Title	N16P_GDDR5_A		
Size	Document Number	LA-H101P	Rev 0.A
Date: Monday, October 22, 2018	Sheet 27 of 53		

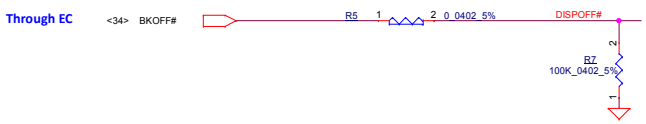
LCD POWER SWITCH



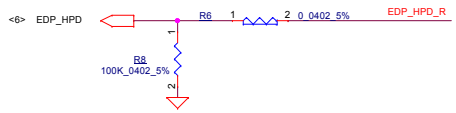
CAMERA POWER CIRCUIT



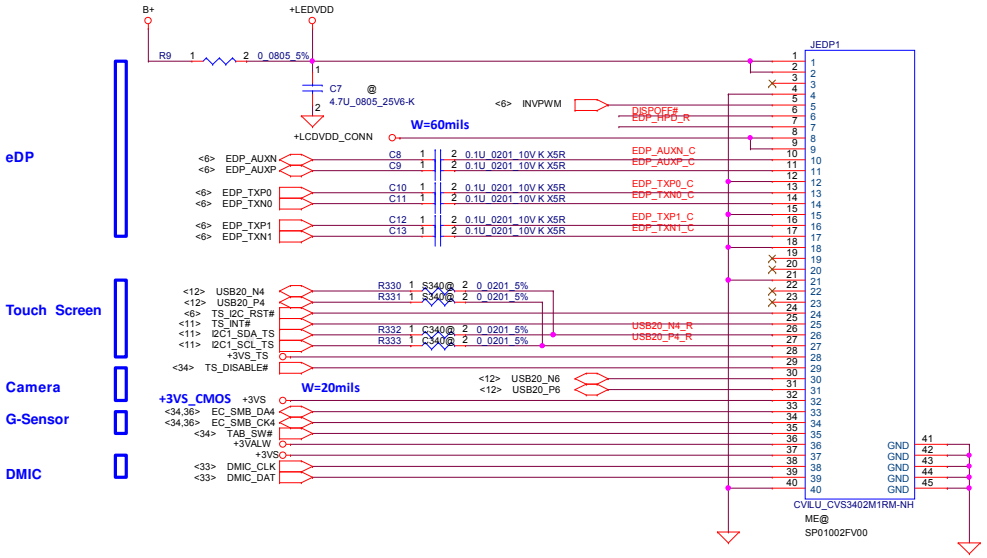
DISPLAY OFF



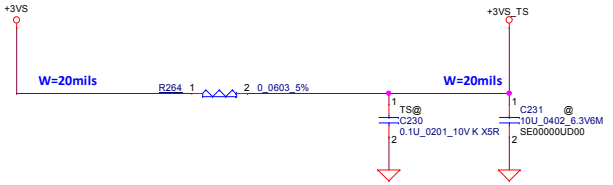
HOT PLUG DETECT



eDP CONNECTOR



Touch Screen POWER CIRCUIT



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Compal Electronics, Inc.			
Title	eDP / Camera / MIC		
Size	Document Number		Rev
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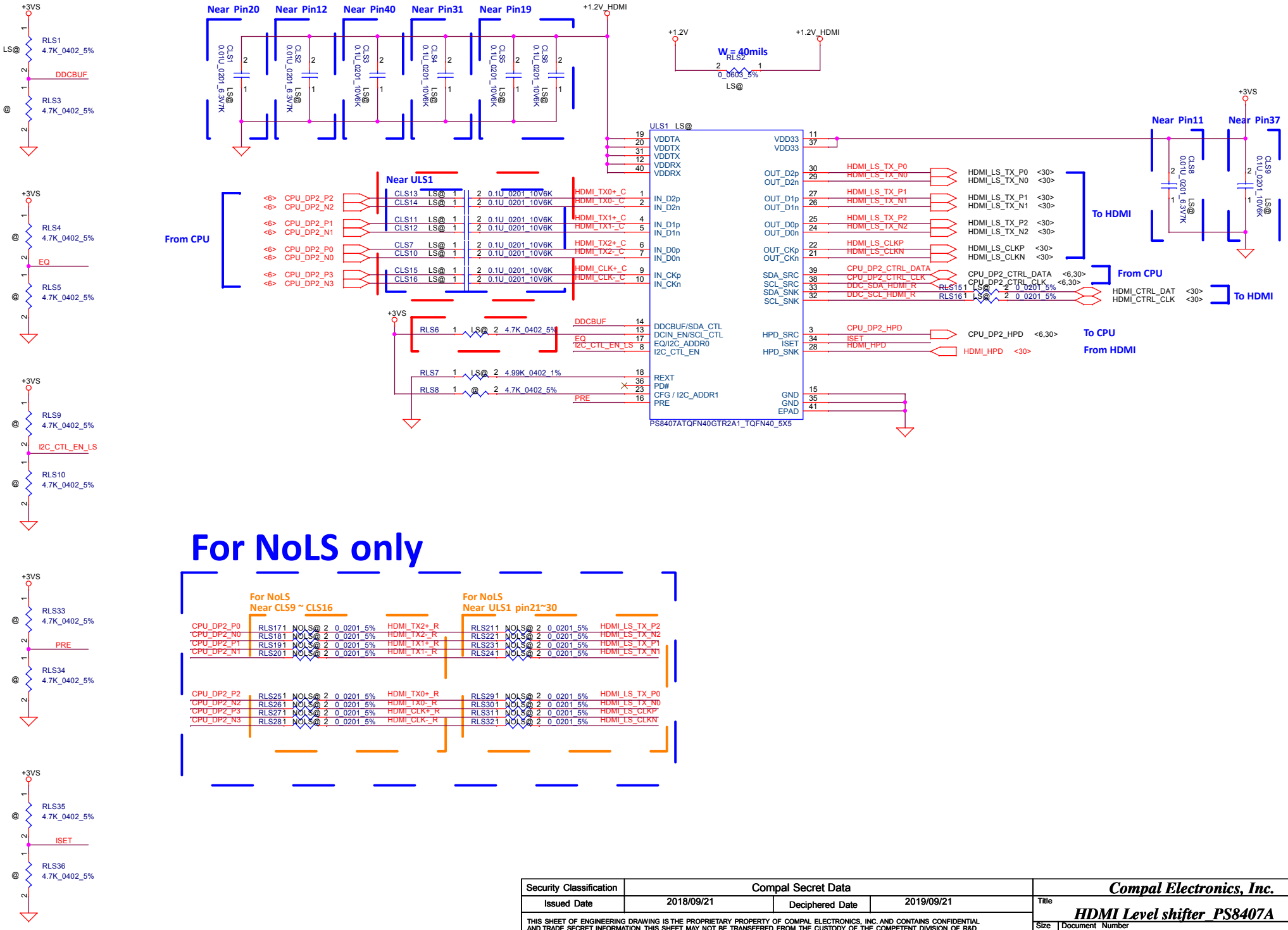
Date:	Thursday, September 20, 2018	Sheet	28 of 51



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Compal Electronics, Inc.		
Title: HDMI Level shifter_PS8407A		
Size	Document Number: LA-H101P	Rev: 0.A
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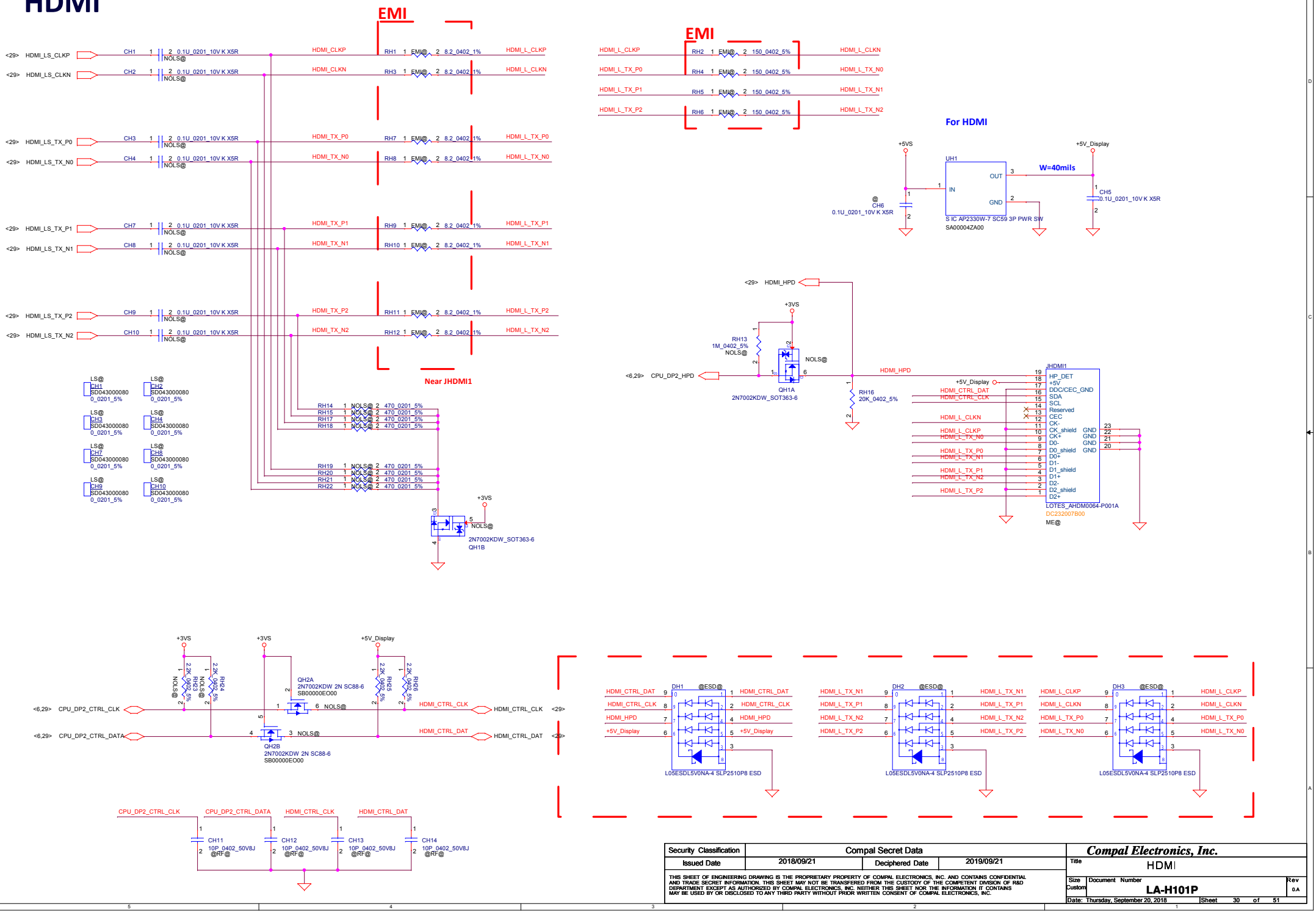
HDMI



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Title: HDMI

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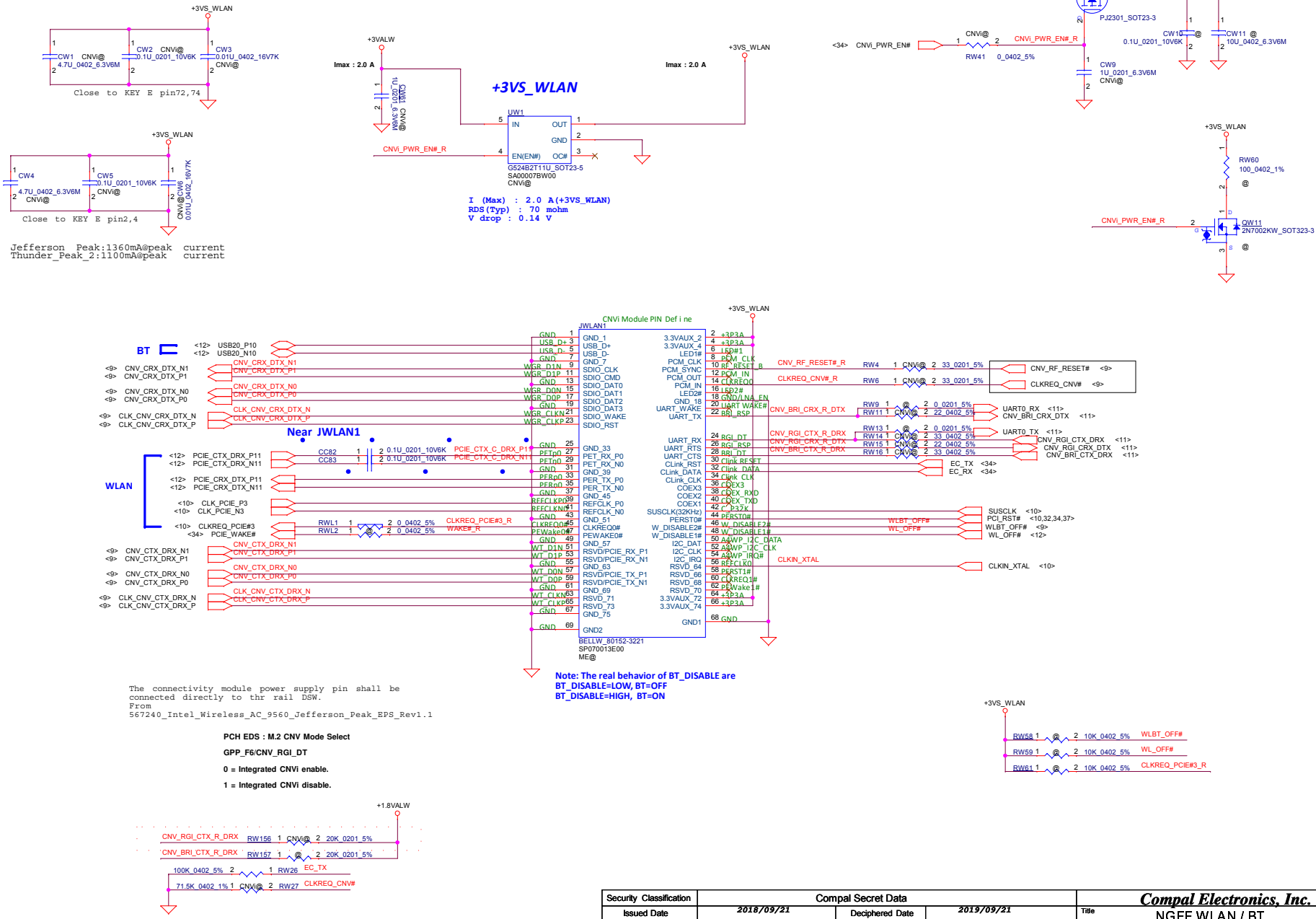
NGFF WLAN /BT(Key E)

NGFF Wireless LAN / BT (Key E) [PCIE+USB/CNVi]



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Title	NGFF WLAN / BT		
Size	Document Number		Rev
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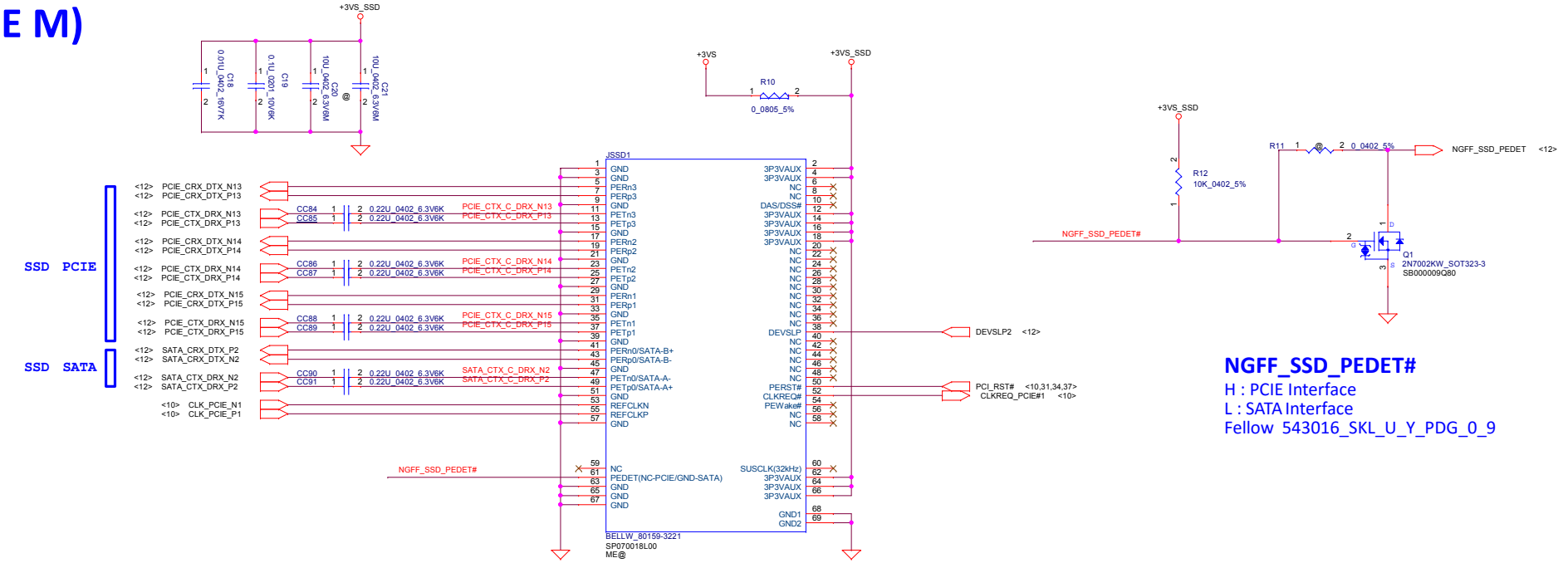
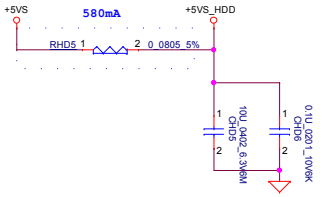
SSD(TYPE M)



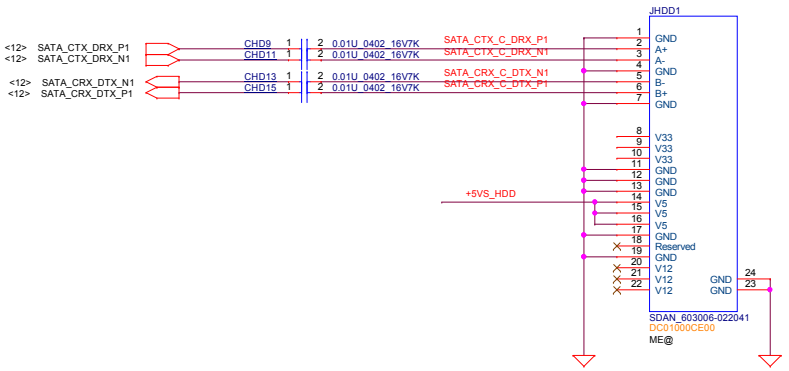
NGFF_SSD_PEDET#
H : PCIE Interface
L : SATA Interface
Fellow 543016_SKL_U_Y_PDG_0_9

SATA HDD

For Power consumption Measurement



SATA HDD Conn.



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Compal Electronics, Inc.

Title	SSD/HDD	
Size: Custom	Document Number: LA-H101P	Rev: 0.A
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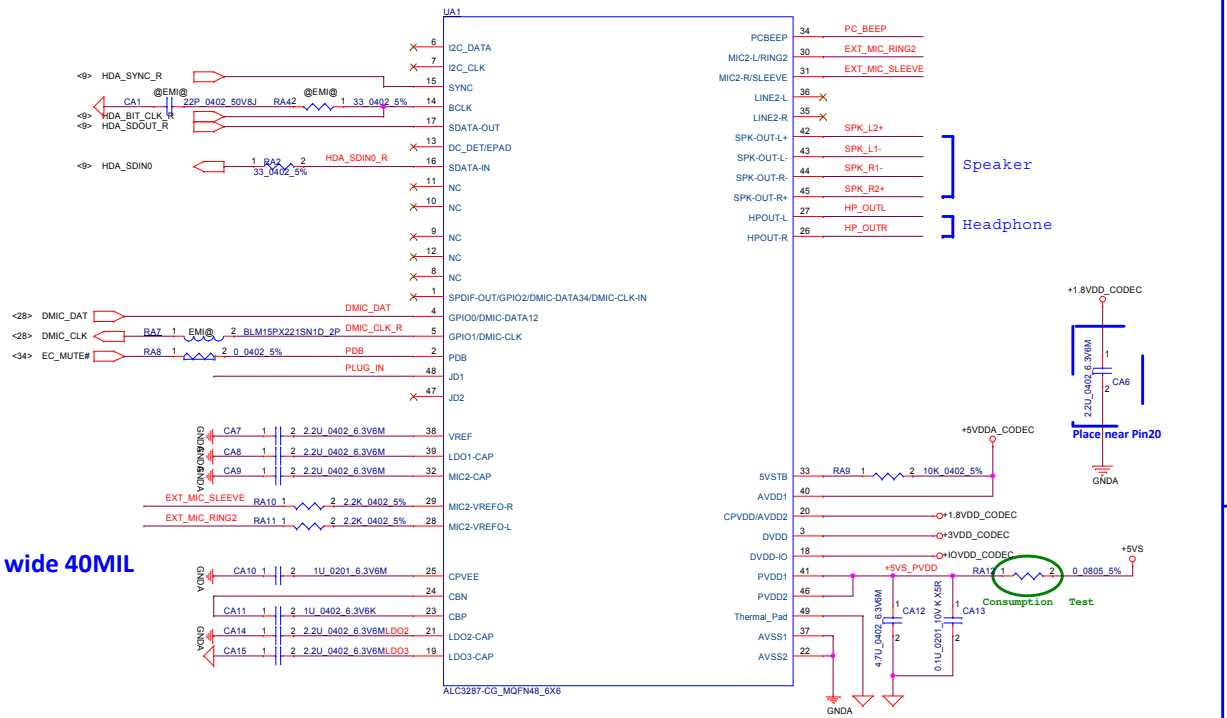
ALC3287



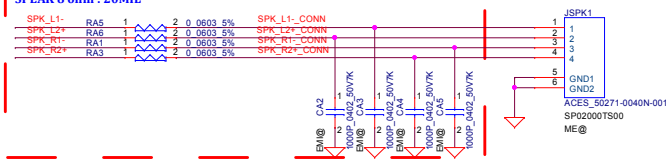
wide 40MIL

Speaker

EMI

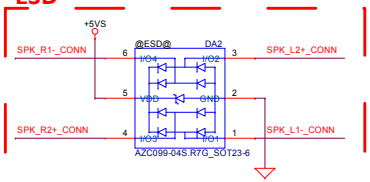
wide 40MIL

SPEAK 4 ohm : 40MIL
SPEAK 8 ohm : 20MIL



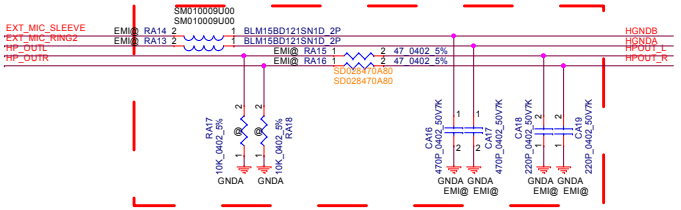
ESD protection needs to be placed near connector side

ESD

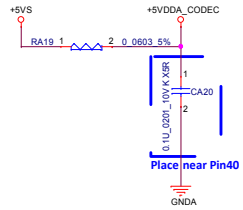


EMI

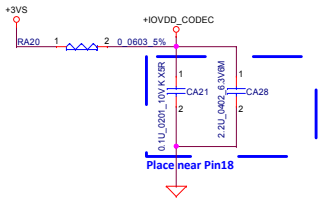
W=40mils
W=40mils



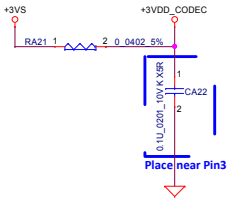
+5VS --> +5VDDA_CODEC



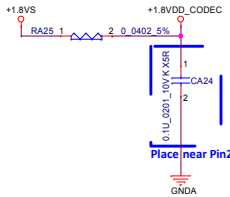
+3.3VS --> +IOVDD_CODEC



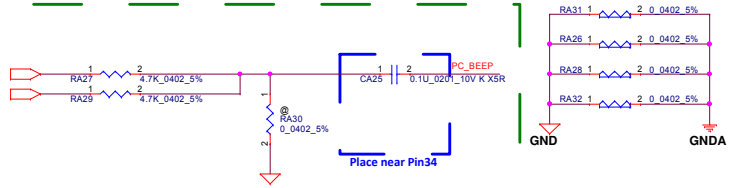
+3VS --> +3VDD_CODEC



+1.8VS --> +1.8VDD_CODEC

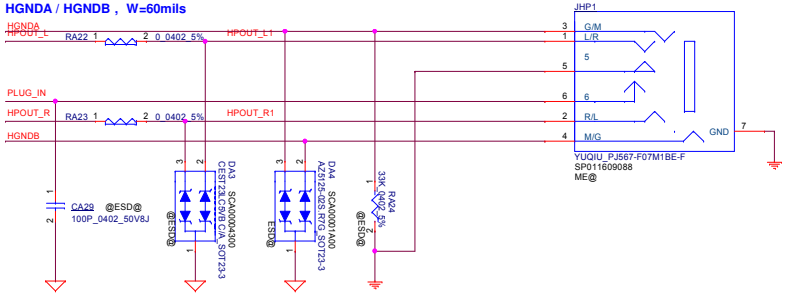


PC Beep



Combo Jack (Normal Open)

HGNDA / HGNDB , W=60mils



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Title: HD Audio Codec_ALC3287

Size: Custom | Document Number: LA-H101P | Rev: 0.A

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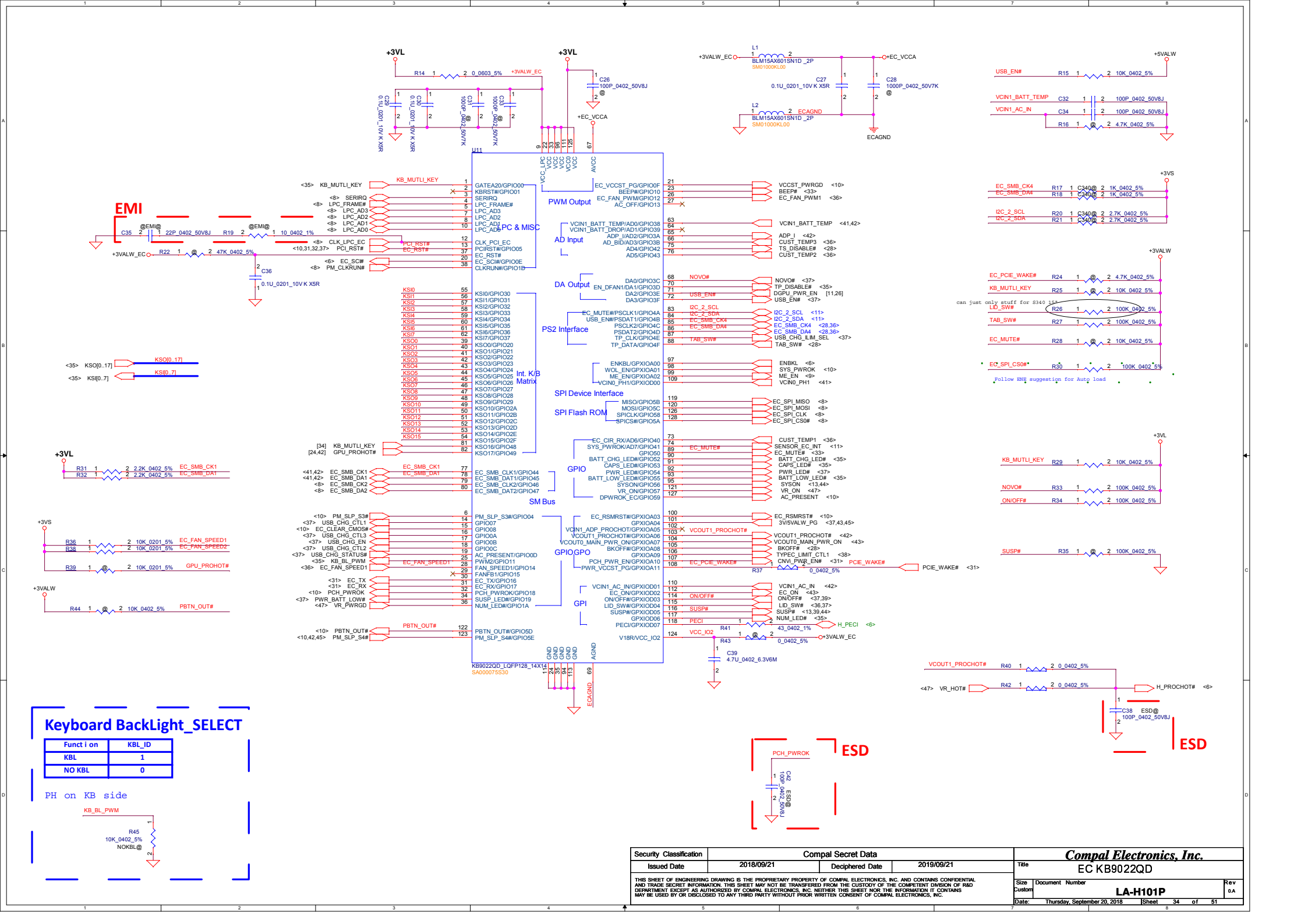

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Compal Electronics, Inc.

Title: EC KB9022QD

Size: Custom | Document Number: LA-H101P | Rev: 0.A

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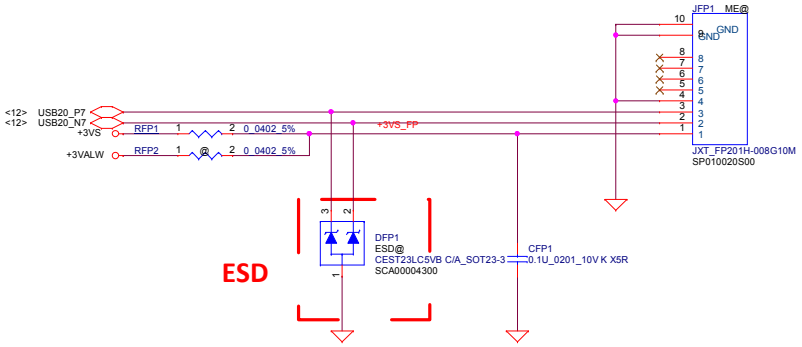
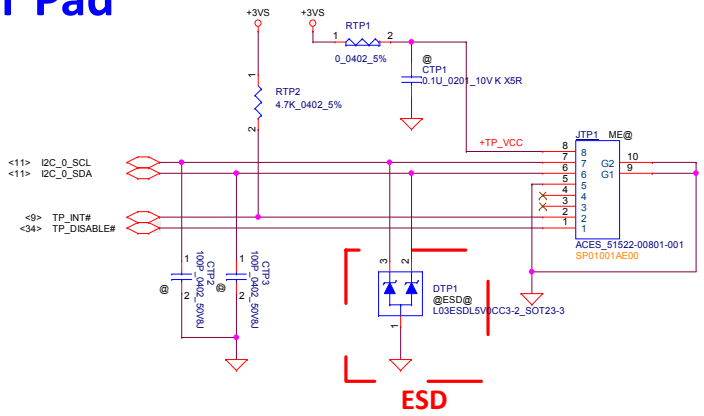
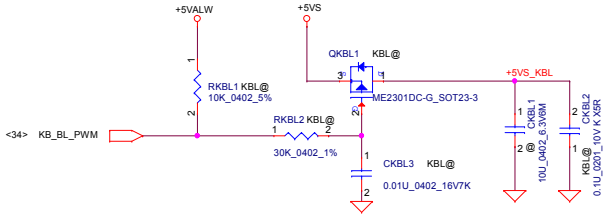
Finger printer



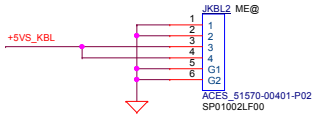
Touch Pad



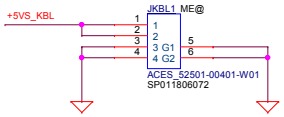
Keyboard Backlight



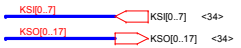
S340-14 & C340-15



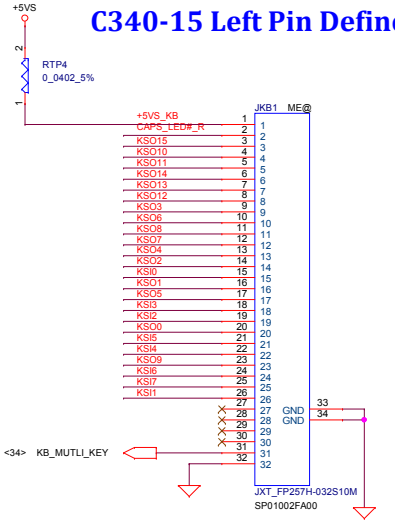
S340-15



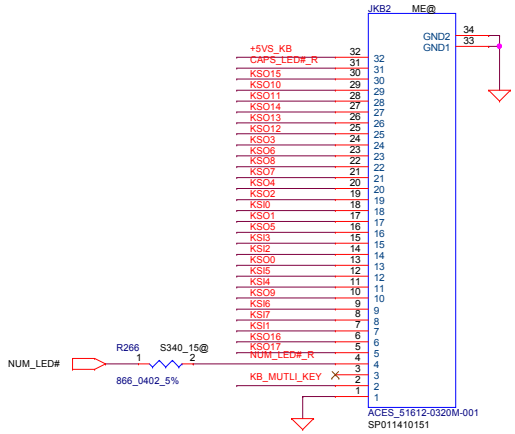
Keyboard

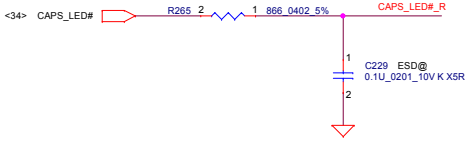


C340-15 Left Pin Define

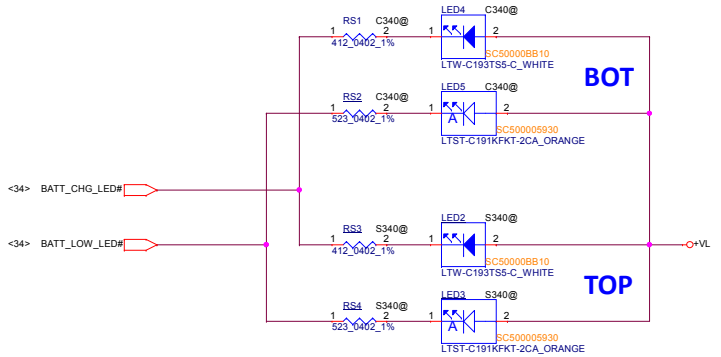


S340-14 & S340-15 Right Pin Define





BATT LED



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Issued Date	2018/09/21	Deciphered Date	2019/09/21

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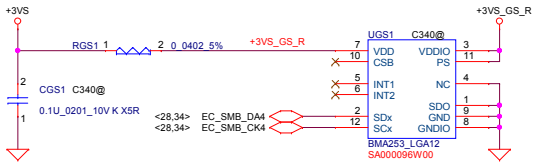
Compal Electronics, Inc.			
Title: KBL/KBD/LED/TP/HS Conn.			
Size: Custom	Document Number: LA-H101P		Rev: 0.A
Date: Thursday, September 20, 2018	Sheet 35 of 51		

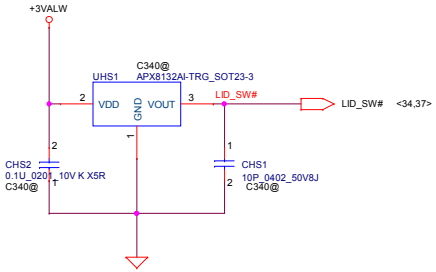
G-Sensor



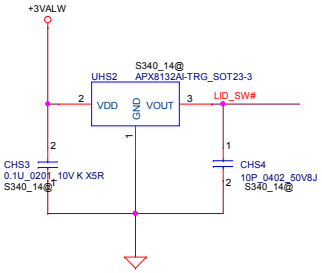
SMB Address: 0X18

Hall Sensor

for C340

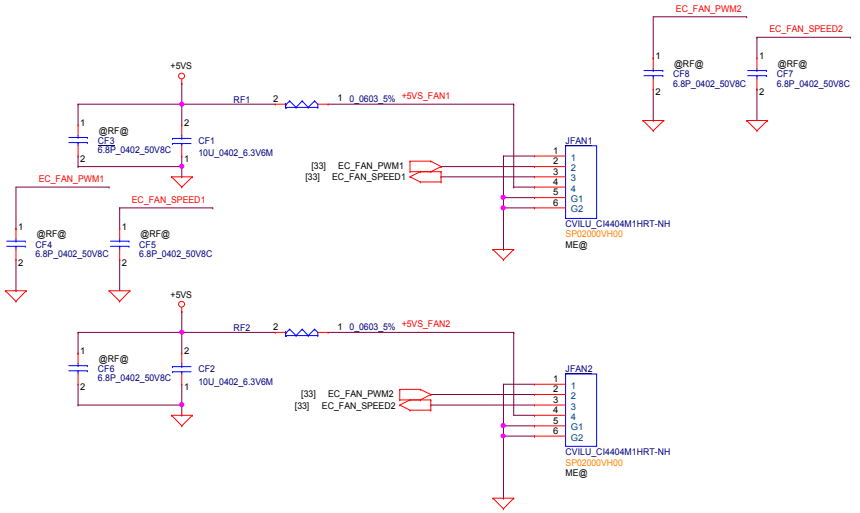


for S340 14"

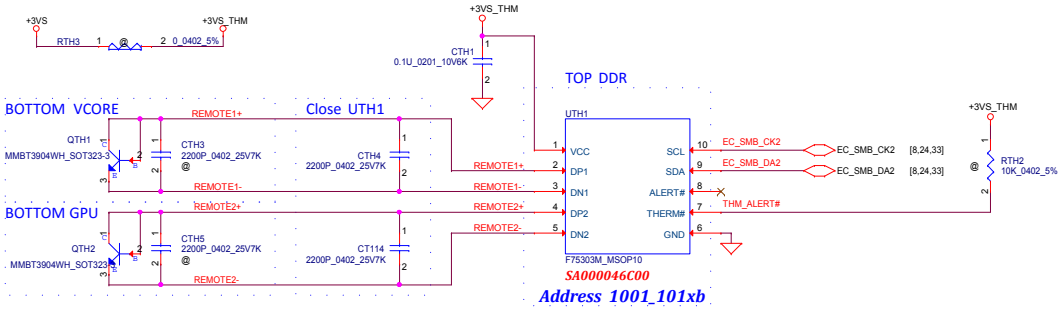


Thermal Sensor

FAN

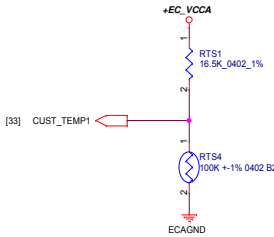


THERMISTOR

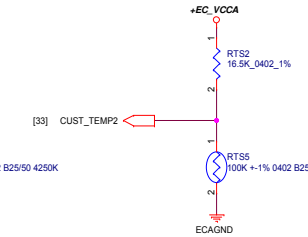


REMOTE1,2 (+/-) :
Trace width/space:10/10 mil
Trace length:<8"

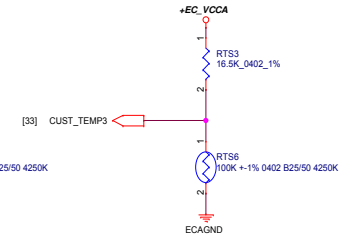
DDR4



GPU_CHOKE



Charger CHOKE



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Issued Date	2018/09/21	Deciphered Date	2019/09/21

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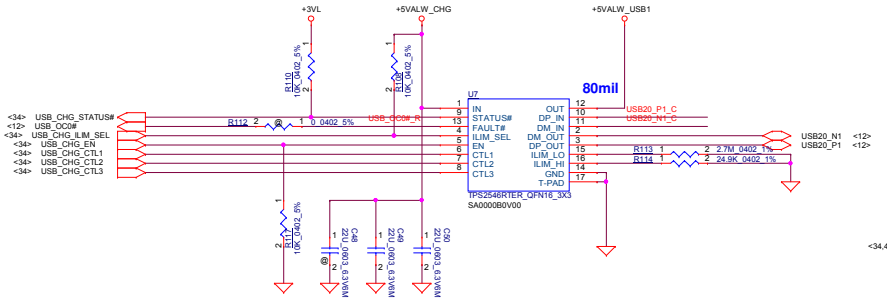
Compal Electronics, Inc.

Title: **FAN / Thermal Senser**

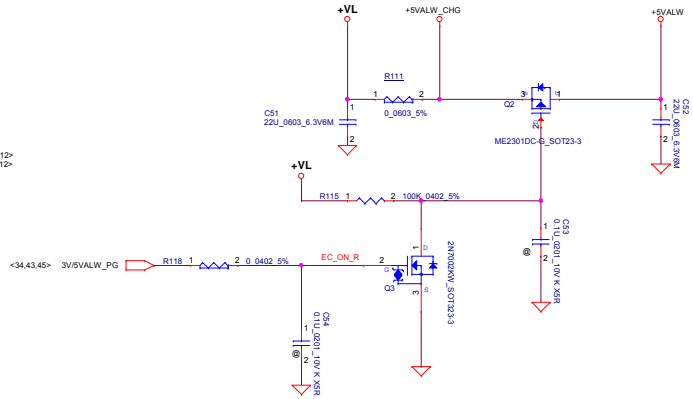
Size	Document Number	Rev
Custom	LA-H101P	0.A

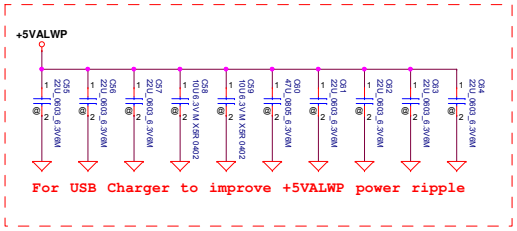
Date: Thursday, September 20, 2018 | Sheet 36 of 51

USB3.0_Port (AOU_Port)

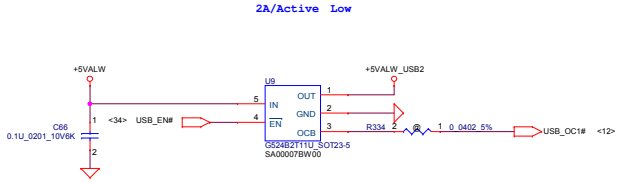


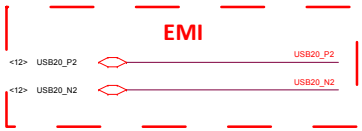
USB Charge switch



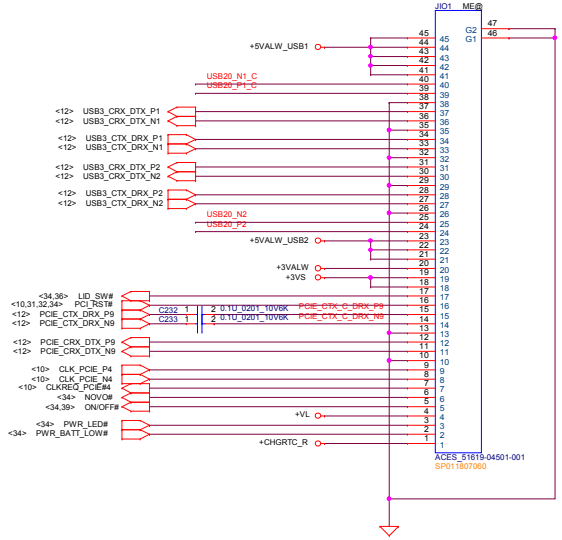


USB3.0_Port (Non-AOU_Port)





I/O CONN



Security Classification	Compal Secret Data		
Issued Date	2018/09/21	Deciphered Date	2019/09/21

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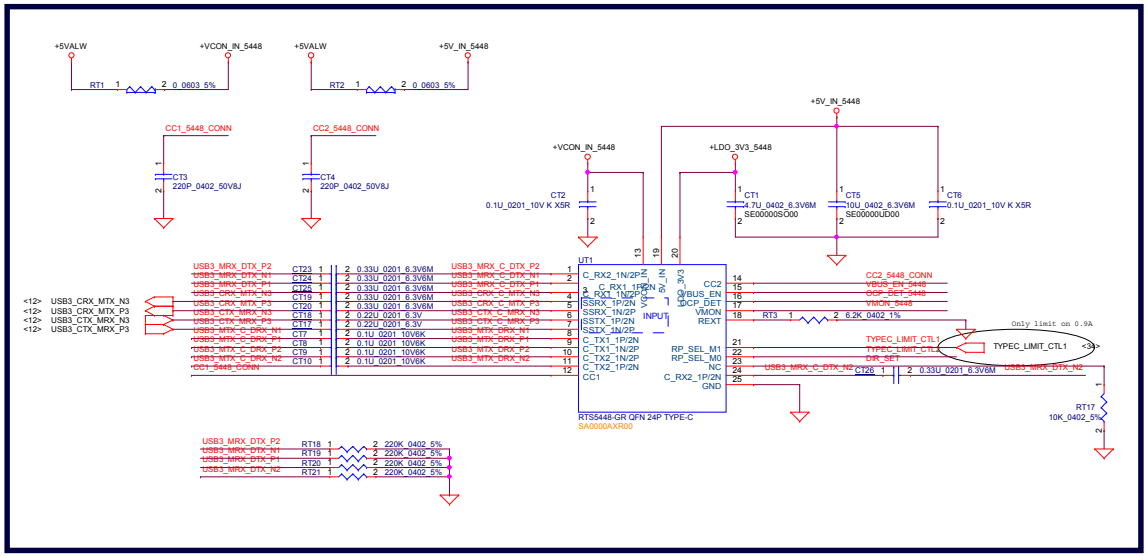
Compal Electronics, Inc.

Title: IO board

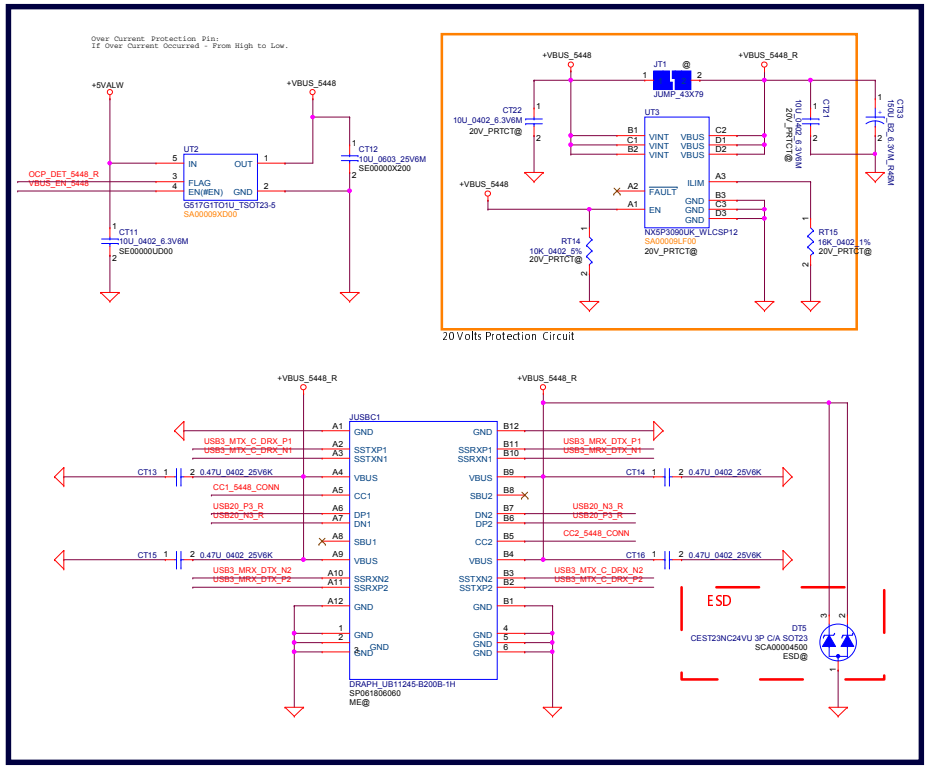
Size: Custom | Document Number: LA-H101P | Rev: 0.A

Date: Thursday, September 20, 2018 | Sheet 37 of 51

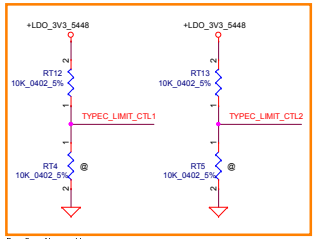
TYPE-C - CC+MUX (RTS5448-GR)



TYPE-C CONNECTOR

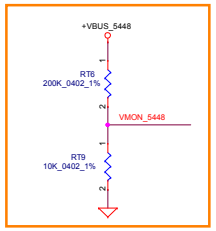


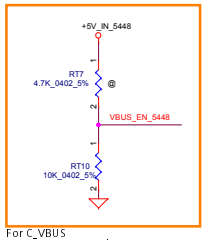
MUX MISC.



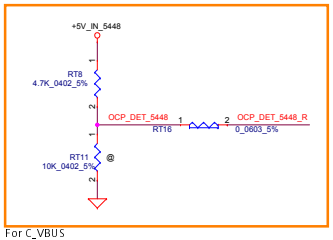
Rp Configuration

	M1	M0	Note
Rp:900mA	0	1	RT4/RT13 mount,RT12/RT5don't mount
Rp:1.5A	1	0	RT12/RT5 mount,RT4/RT13don't mount
Rp:3.0A	1	1	RT12/RT13mount,RT4/RT5 don't mount





For C_VBUS
(Power Switch Enable Pin)

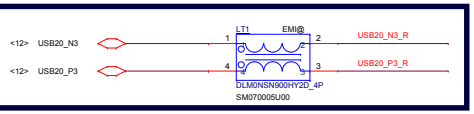


For C_VBUS
(Power Switch OCP Pin)

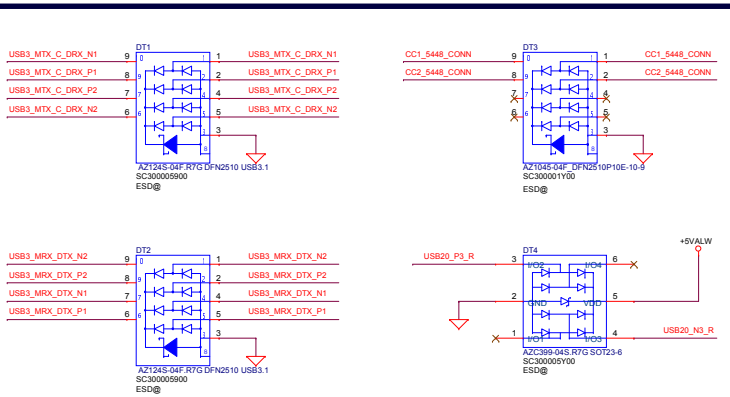
Power switch enable pin	Note
Low Active	RT7/RT10 mount
High Active	RT10 mount, RT7 don't mount

Power switch OCP pin	Note
Low Active	RT8/RT11 mount
High Active	RT11 mount, RT8 don't mount

USB2.0



ESD COMPONENTS



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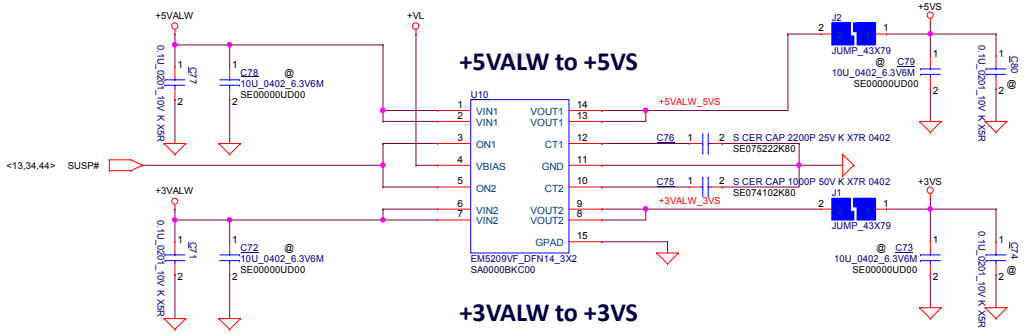
Compal Electronics, Inc.

Title: Type-C

Size: Custom | Document Number: LA-H101P | Rev: 0.A

Date: Thursday, September 20, 2018 | Sheet 38 of 51

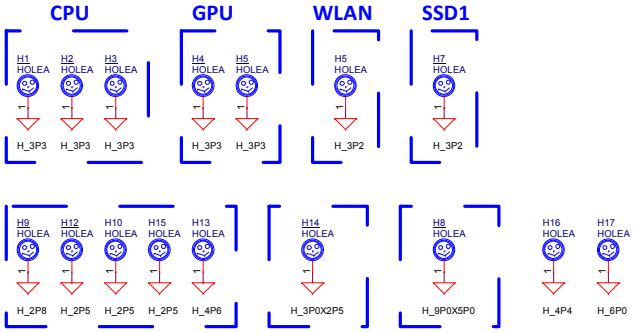
DC to DC

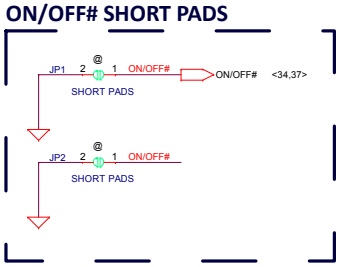


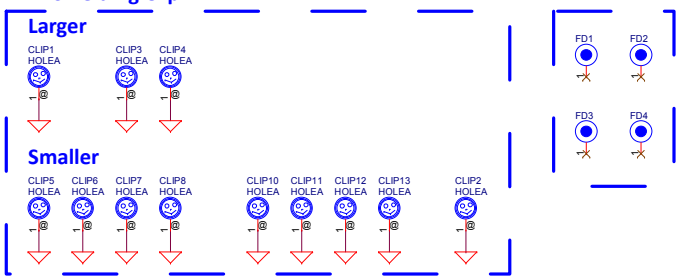
DISCHARGE CIRCUIT

For +1.8VALW Discharge

MISC.







Security Classification	Compal Secret Data		
Issued Date	2018/09/21	Deciphered Date	2019/09/21

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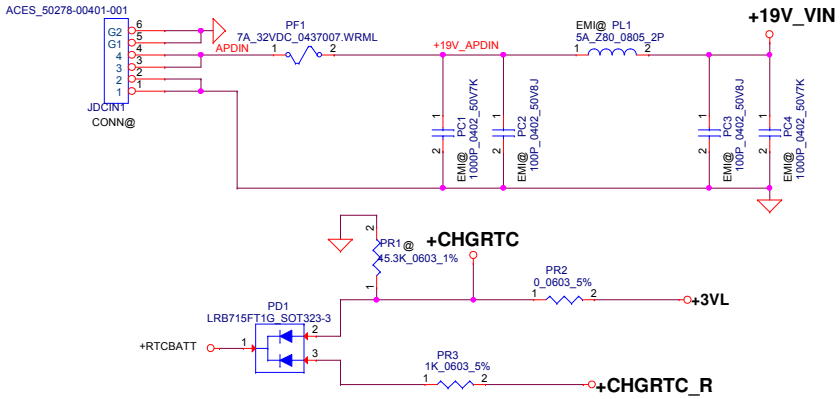
Compal Electronics, Inc.			
Title	DC to DC / Discharge / MISC		
Size	Document Number		Rev
Custom	LA-H101P		0.A
Date:	Thursday, September 20, 2018	Sheet	39 of 51



Security Classification	Compal Secret Data		
Issued Date	2018/04/09	Deciphered Date	2019/04/09

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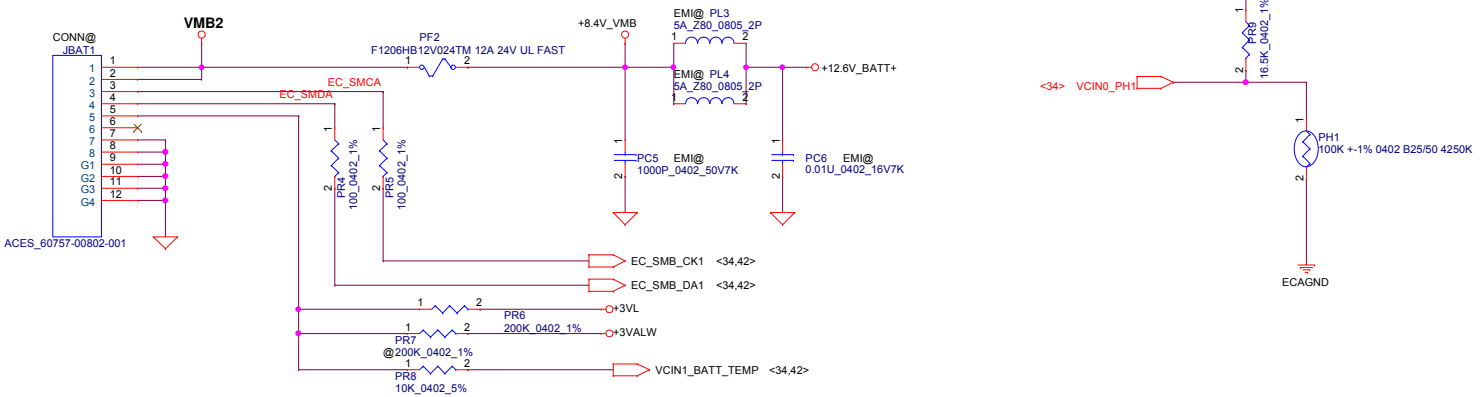
Compal Electronics, Inc.

Title: **PWR- DCIN / Vin Detector**

Size	Document Number	Rev
Custom	*LA-H101P*	0.A

Date: Thursday, September 20, 2018 Sheet 40 of 54

PH201 under CPU botten side :
CPU thermal protection at 93 +-3 degree C
Recovery at 56 +-3 degree C



Security Classification	Compal Secret Data		
Issued Date	2018/04/09	Deciphered Date	2019/04/09

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Compal Electronics, Inc.

Title: **PWR- BATTERY CONN/OTP**

Size	Document Number	Rev
Custom	*LA-H101P*	0.A

Date: Thursday, September 20, 2018 Sheet 41 of 54

Module model information

ISL95520A_Hybrid_Boost_V2.mdd

Protection for reverse input

Vgs = 20V
Vds = 60V
Id = 250mA

PQ314 S TR 2N7002KW 1N SOT323-3

Rds(on) = 15.8mohm max
Vgs = 20V
Vds = 30V
ID = 10.5A (Ta=70C)

max Power loss 0.22W for 90W;0.12W for 65W system;0.05W for 45W
CSR rating: 1W
VCSIP-VCSIN spec < 81mV

Need check the SOA for inrush

+19V_VIN

PR301 1M_0402_1%

PR302 3M_0402_5%

PQ311 EMB04N03H 1N EDFN5X6-8

+19V_P1

PQ312 AON7506_DFN33-8-5

+19V_P2

PR303 0.01_1206_1%

B+

PC301 10U_0603_25V6M

PC302 10U_0603_25V6M

PC303 0.1U_0402_25V6

PC304 2200P_0402_25V7K

PR306 287K_0402_1%

ASGATE_CHG_R

CSIP_CHG_R

CSIN_CHG_R

PR304 0_0402_5%

PR305 2_0402_5%

@PC323 0.1U_0402_25V6

PC305 0.1U_0402_25V6

@PC324 0.1U_0402_25V6

PR307 4.02K_0402_1%

PR308 4.02K_0402_1%

PR309 100_0402_1%

+12.6V_BATT+

PR729 and PR732 are ACDET set ting base on your project to set

PR310 49.9K_0402_1%

PC306 2200P_0402_50V7K

CMSRC_CHG

ASGATE_CHG

PC307 0.22U_0603_25V7K

Rds(on) = 32mohm max
Vgs = 20V
Vds = 30V
ID = 8A (Ta=70C)

PQ313 AON7506_DFN33-8-5

PC308 0.1U_0402_25V6

support Turbo boost : 2200P
no support Turbo boost : 0.1u

0x3CH <BIT9> PSYS current gain
Rs1 = 10mΩ and Rs2 = 5mΩ or Rs1 = 10mΩ and Rs2 = 10mΩ
BIT0 = 1.14uA/W
BIT1 = 0.285uA/W
==========
Rs1 = 20mΩ and Rs2 = 10mΩ or Rs1 = 20mΩ and Rs2 = 20mΩ
BIT0 = 2.28uA/W
BIT1 = 0.57uA/W

Ipsys = KPSYS x (VAD P x IAD P + VBA T x IBE T)
R_Psys = 1.2V / Ipsys
KPSYS = 1.14uA/W
adapter wattage = 45W
Battery wattage = 40Wh
Ipsys = 1.14 x (45÷40) = 96.9uA
R_Psys = 1.2V / 96.9uA = 12.3K-ohm.
==========
adapter wattage = 65W
Battery wattage = 40Wh
Ipsys = 1.14 x (65÷40) = 119.7uA
R_Psys = 1.2V / 96.9uA = 10K-ohm.

PR311 100K_0402_1%

PR314 158K_0402_1%

<34> VCIN1_AC_IN

<34,41> EC_SMB_DA1

<34,41> EC_SMB_CK1

<34> VCOUT1_PROCHOT#

<34> ADP_I

PR312 0_0402_5%

PR320 0_0402_5%

PR316 1K_0402_1%

PR318 1K_0402_1%

PR321 1K_0402_1%

AMON_ISL95520

BMON_ISL95520

Close to EC.

PU301 ISL95520AHRZ-T_QFN32_4X4

ACIN
ACOK
SDA
SCL
PROCHOT#
AMON
BMON
PSYS
CSIP
CSIN
ASGATE
CMSRC
OPCN
OPCP
VBAT
BGATE
BOOT
UGATE
PHASE
LGATE
VDDP
VDD
DCIN
NTC
AGND
PROG
COMP
CCLIM
FSET
BATGONE
CSON
CSOP
ACLIM

PC316 0.1U_0402_25V6

PC317 0.1U_0402_25V6

Close to EC.

Follow adapter and battery wattage in Vsys current source.
Base on CPU Core VR design.
The resistor is pop on CPU VR schematic.

PR313 0_0603_5%

PC309 0.22U_0603_25V7K

BST_CHG

UG_CHG

LX_CHG

LG_CHG

VDDP_CHG

VDD_CHG

PQ301 AON7408L_DFN8-5

7X7X3
Isat: 6.5A
DCR: 28mohm

PL301 4.7UH_5.5A_20%_7X7X3_M

+12.6V_BATT_CHG

PR315 0.01_1206_1%

+12.6V_BATT+

PC310 10U_0603_25V6M

PC311 10U_0603_25V6M

PC312 10U_0603_25V6M

PC322 10U_0603_25V6M

PQ302 AON7506_DFN33-8-5

PR319 4.7_0402_5%

PC313 1U_0402_16V6K

PC314 1U_0402_16V6K

PR323 100K_0402_1%

PR324 10_1206_5%

PD301 LRB715FT1G_SOT323-3

+19V_VIN

BA

VF = 0.38V

PR318 1U_0603_25V6

A31 connect to BA
Other team connect to bat t conn

PQ315 LMUN5113T1G_SOT323-3

PQ316 LTC015EUBFS8TL_UMT3F

<10,34,45> PM_SLP_S4#

PR325 10K_0402_1%

VDD=5V

VDD_CHG

CCLIM_CHG

ACLIM_CHG

PROG_CHG

COMP_CHG

FSET_CHG

PR326 200K_0402_1%

PR327 200K_0402_1%

PR335 348K_0402_1%

PR334 76.8K_0402_1%

PR333 182K_0402_1%

PC320 560P_0402_50V7K

PR330 499_0402_1%

PR331 38.3K_0402_1%

PC321 0.015U_0402_25V7K

Fs=729KHZ ~ +/- 15%

CSOP_CHG

CSOP_CHG_R

PR328 2_0402_5%

PC319 0.1U_0402_25V6

CSON_CHG

CSON_CHG_R

PR332 0_0402_5%

VCIN1_BATT_TEMP <34,41>

BATGONE(BATT_TEMP)
logic high: above 2.4V
logic low: under 0.8V

Hybrid boost power mode
Cell = 3s

Support max charge 3.5A
Power loss: 0.245W
CSR rating: 1W
VCSPP-VCSON spec < 81mV

For A31 only.
Turn off Charger IC on battery only.
Depend on customer design for system power consumption.

Design Notes
For 45W/65W /90W system, 2S/3S/4S battery
Maximum Charging current 3.5A
Maximum Battery discharge power 55W
#Register Setting
1. OX3DH bit10 set 0 (default 1) to enable turbo boost function
2. Disable turbo when AC only
#Circuit Design
1. ACLIM and CCLIM are devider voltage control.
2. Use 7X7 choke and 3X3 H/L side MOSFET
Charge current 3A
Power loss : 1.79W (H/S=0.227W,L/S=1.2738W,Choke=0.297W)
Power density : 0.61 (23X16)
#Protect function
1. ACOVP : VCC voltage > 24V
2. SMBus timeout : OX3DH bit15 set 0 (default 0) to enable 175s(default).
3. ACOC : OX3CH bit4 set1 release adapter limit function (default:Enable).
4. CHGOCP : based on charge current setting
5. BATOVP : 4.6V/Cell
6. BATLOWV : No.
7. TSHUT : 150C

(Rs1 = 10mΩ and Rs2 = 5mΩ or Rs1 = 20mΩ and Rs2 = 10mΩ).
CC_LIM = VccLIM / 64 x Rs2
==========
(Rs1 = 10mΩ and Rs2 = 10mΩ or Rs1 = 20mΩ and Rs2 = 20mΩ)
CC_LIM = VccLIM / 32 x Rs2
==========
AC_LIM = Vac_LIM / 32 x Rs1

Battery current limimed by CCLIm ~ 3.89A.
Adapter current limimed by ACLIm ~ 4.33A.
(PR779 and PQ741 are for change ACLIm when AC in)

+3VS

Pull high on HW side

VGA@ PR1681 10K_0402_5%

VGA@ PR1680 10K_0402_5%

VGA@ PQ1660A

GPU_PROHOT# [24,33]

2N7002KDW_SOT363-6

[33,42] VCOUT1_PROCHOT#

VGA@ PQ1661 SSM3K35MFV 1N VESM

VGA@ PQ1660B

[33,42] VCIN1_AC_IN

2N7002KDW_SOT363-6

Security Classification	Compal Secret Data		
Issued Date	2014/11/05	Deciphered Date	2014/12/15

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Compal Electronics, Inc.

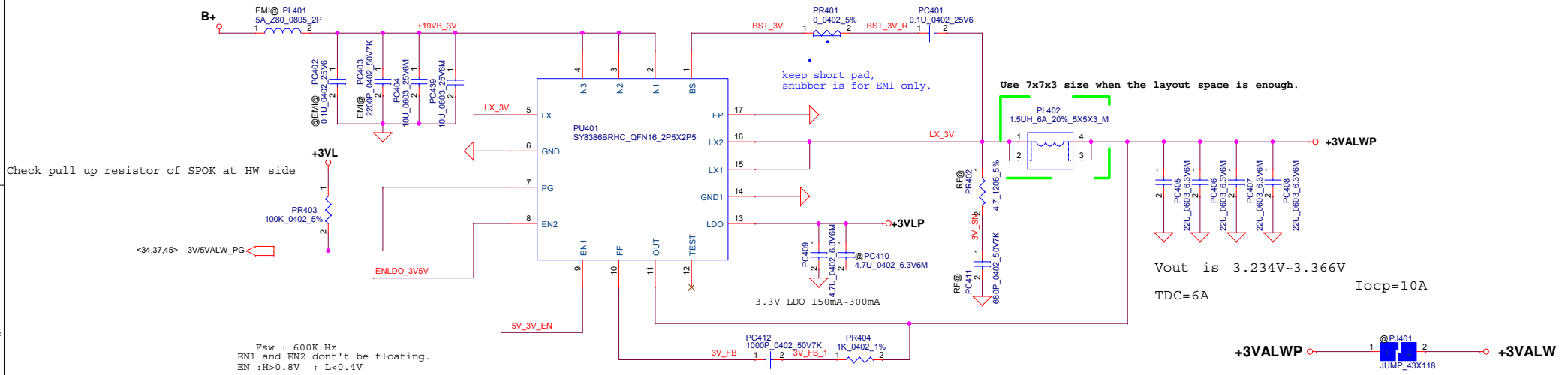
Title: PWR_CHARGER

Size: | Document Number: LA-H101P | Rev: 0.A

Date: Thursday, September 20, 2018 | Sheet 42 of 54

Module model information

SY8286B_V3_single.mdd
SY8286B_V3_dual.mdd

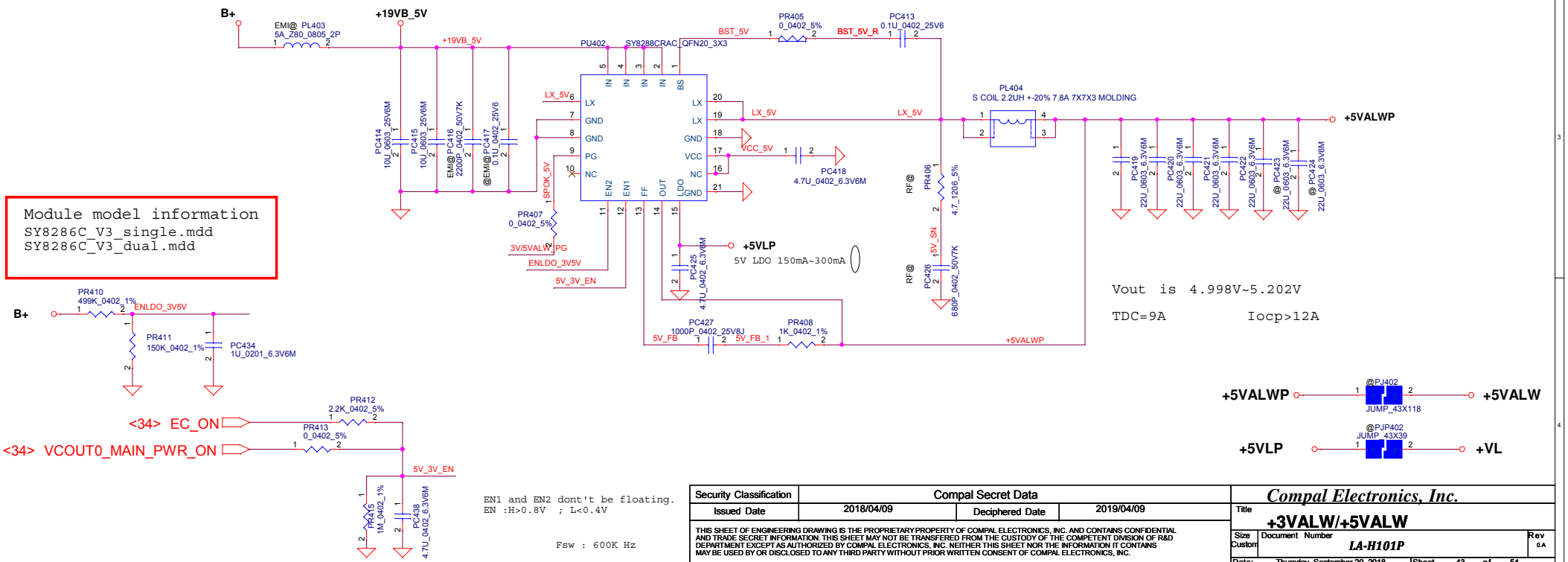


+3VALWP — @PJ401 JUMP_43X118 — +3VALW

+3VLP — @PJP401 JUMP_43X39 — +3VL

Module model information

SY8286C_V3_single.mdd
SY8286C_V3_dual.mdd



+5VALWP — @PJ402 JUMP_43X118 — +5VALW

+5VLP — @PJP402 JUMP_43X39 — +VL

Security Classification	Compal Secret Data		
Issued Date	2018/04/09	Deciphered Date	2019/04/09

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Compal Electronics, Inc.

Title: +3VALW/+5VALW

Size	Document Number	Rev
Custom	LA-H101P	0.A

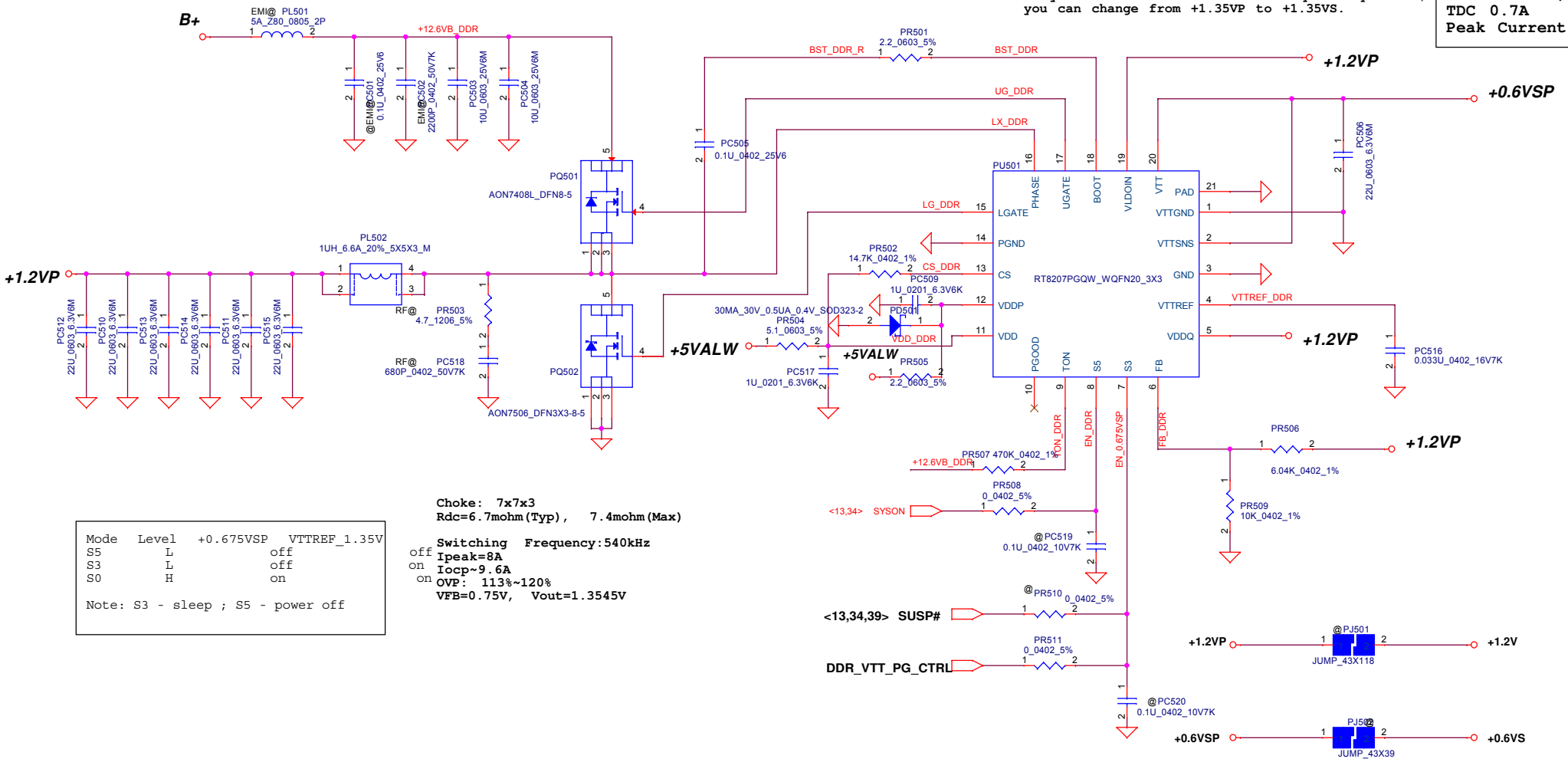
Date: Thursday, September 20, 2018 | Sheet 43 of 54

Module model information

RT8207P_single_V3.mdd For Single layer
RT8207P_dual_V3.mdd For Dual layer

Pin19 need pull separate from +1.35VP.
If you have +1.35V and +0.675V sequence question, you can change from +1.35VP to +1.35VS.

0.675Volt +/- 5%
TDC 0.7A
Peak Current 1A



Mode	Level	+0.675VSP	VTTREF_1.35V
S5	L	off	
S3	L	off	
S0	H	on	

Note: S3 - sleep ; S5 - power off

Choke: 7x7x3
Rdc=6.7mohm(Typ), 7.4mohm(Max)

Switching Frequency:540kHz
Ipeak=8A
Iocp~9.6A
OVP: 113%~120%
VFB=0.75V, Vout=1.3545V

Security Classification	Compal Secret Data		
Issued Date	2018/04/09	Deciphered Date	2019/04/09

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Compal Electronics, Inc.

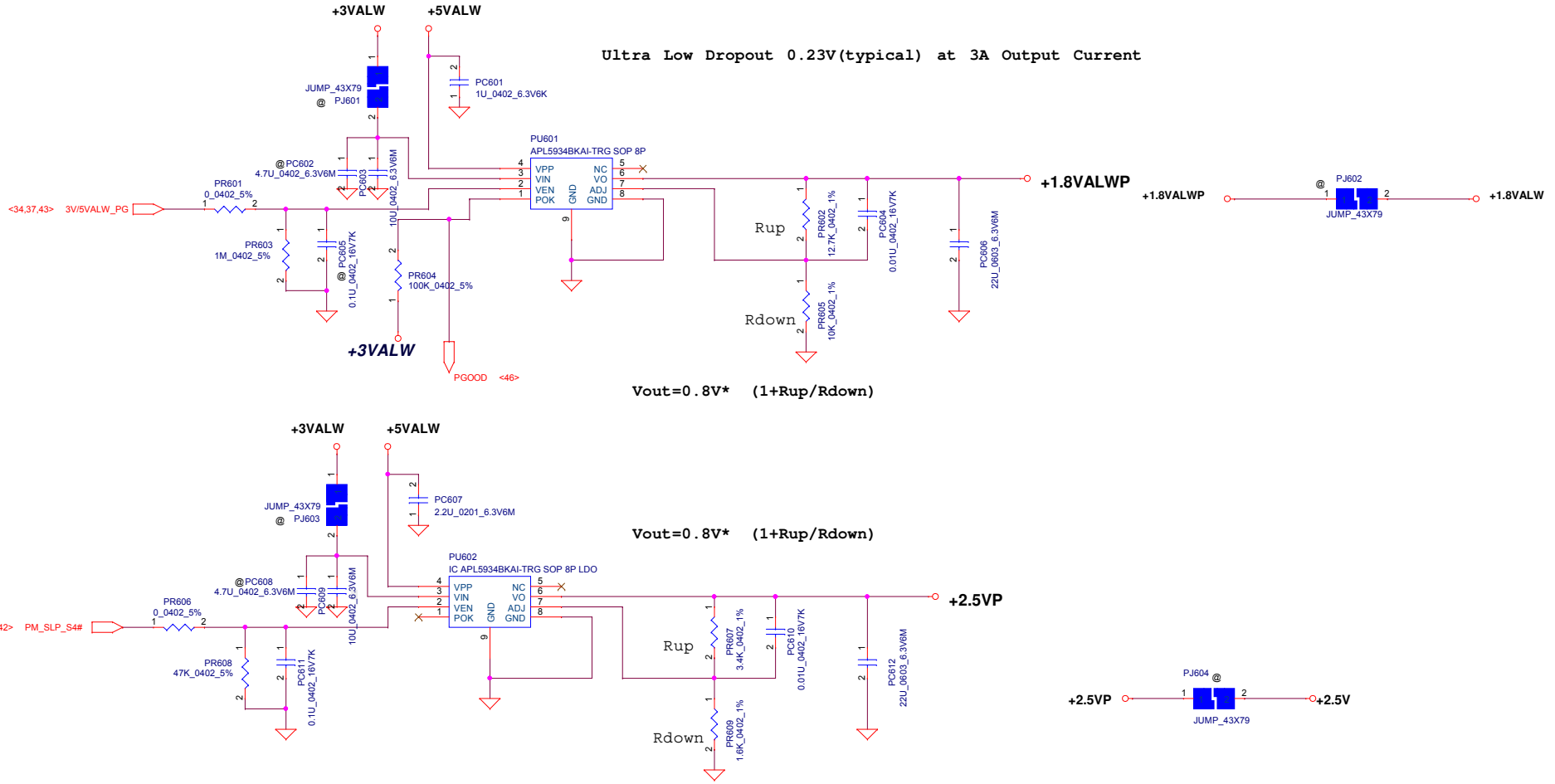
Title: RT8207P

Size: Custom | Document Number: LA-H101P | Rev: 0.A

Date: Thursday, September 20, 2018 | Sheet 44 of 54

Module model information

APL5930_V2.mdd



Security Classification	Compal Secret Data		
Issued Date	2018/04/09	Deciphered Date	2019/04/09

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Compal Electronics, Inc.

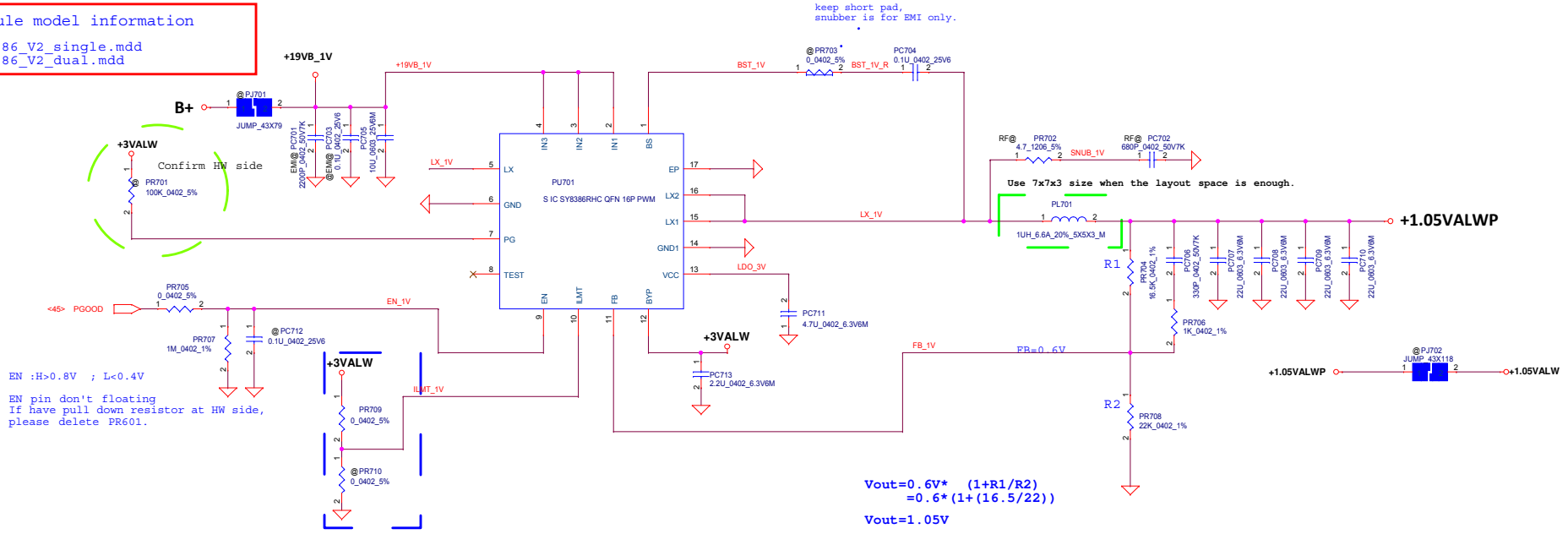
Title: APL5930

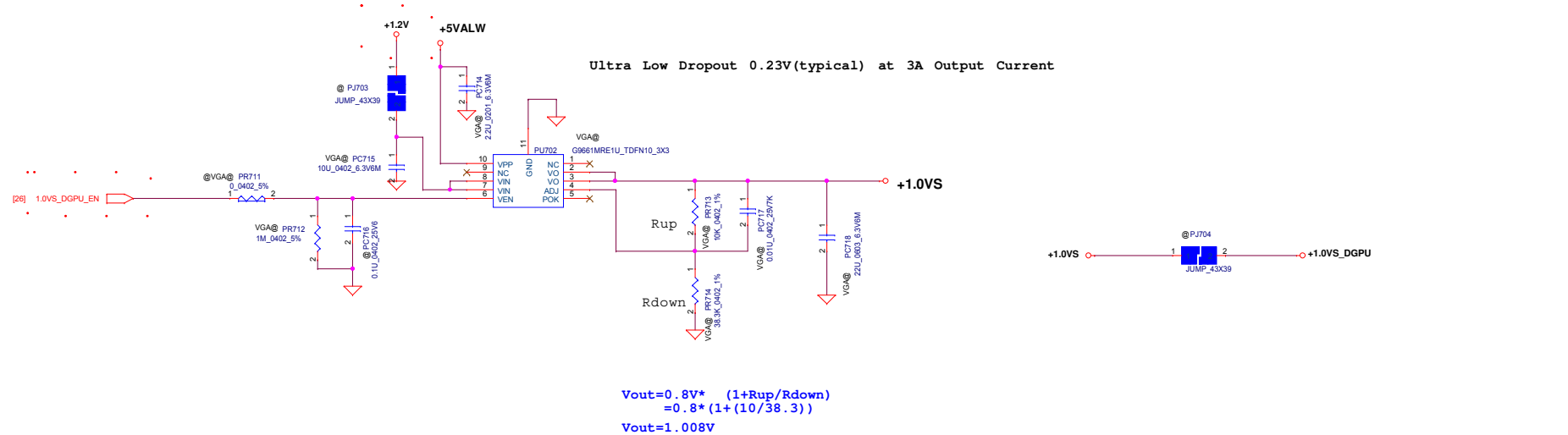
Size	Document Number	Rev
Custom	LA-H101P	0.A

Date: Thursday, September 20, 2018 Sheet 45 of 54

Module model information

SY8286_V2_single.mdd
SY8286_V2_dual.mdd





Security Classification	Compal Secret Data		
Issued Date	2018/04/09	Deciphered Date	2019/04/09

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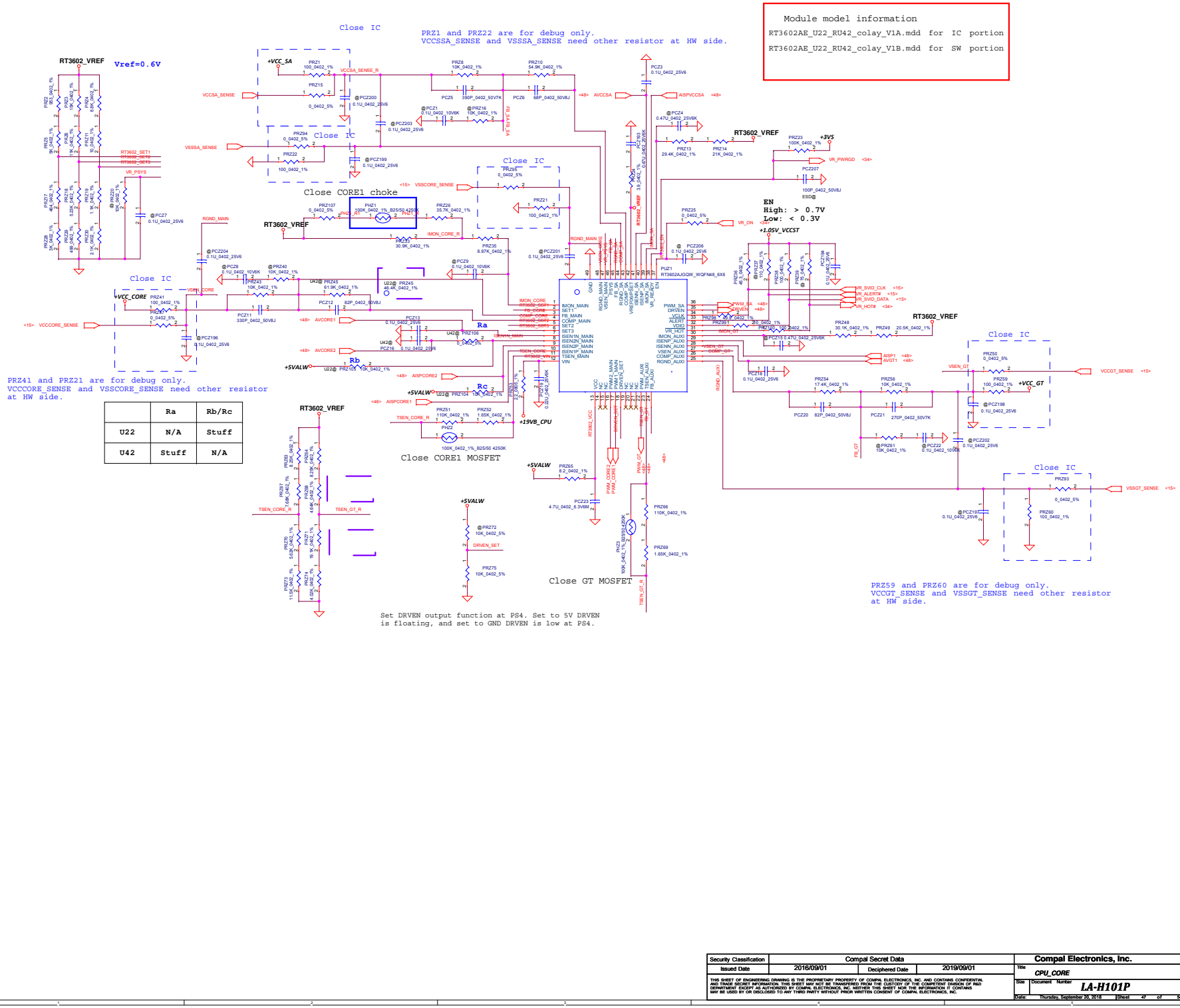
Compal Electronics, Inc.

Title: SY8286

Size: C | Document Number: LA-H101P | Rev: 0.A

Date: Thursday, September 20, 2018 | Sheet 46 of 54



	Ra	Rb/Rc
U22	N/A	Stuff
U42	Stuff	N/A

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2016/09/01	Deciphered Date	2019/09/01

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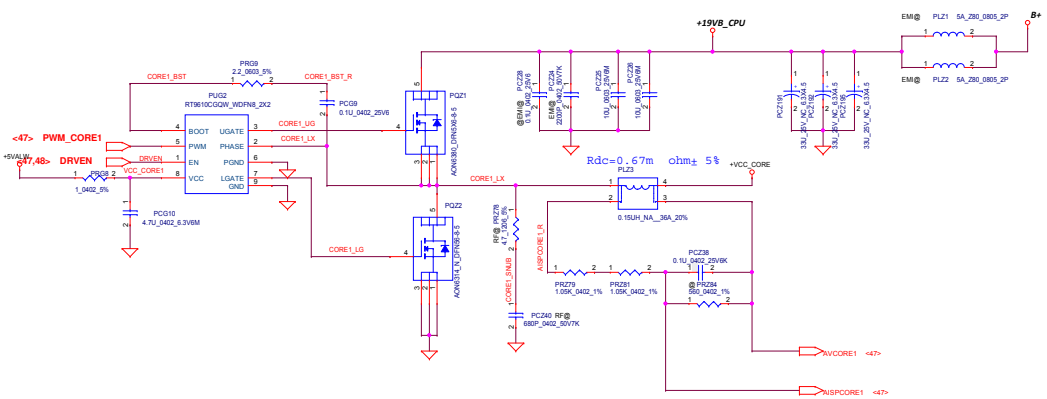
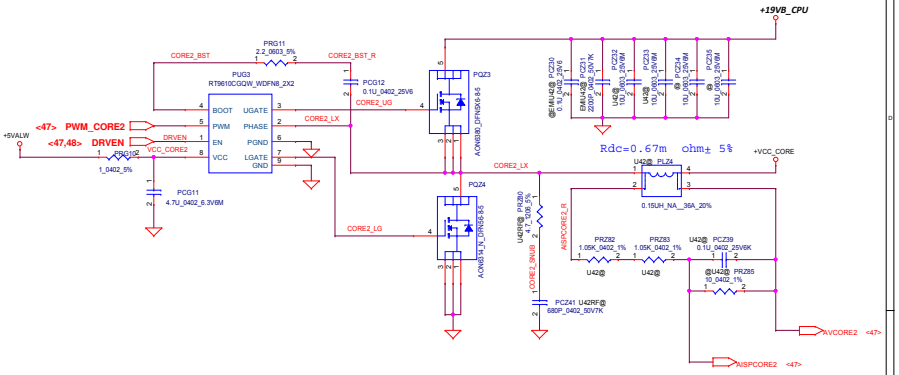
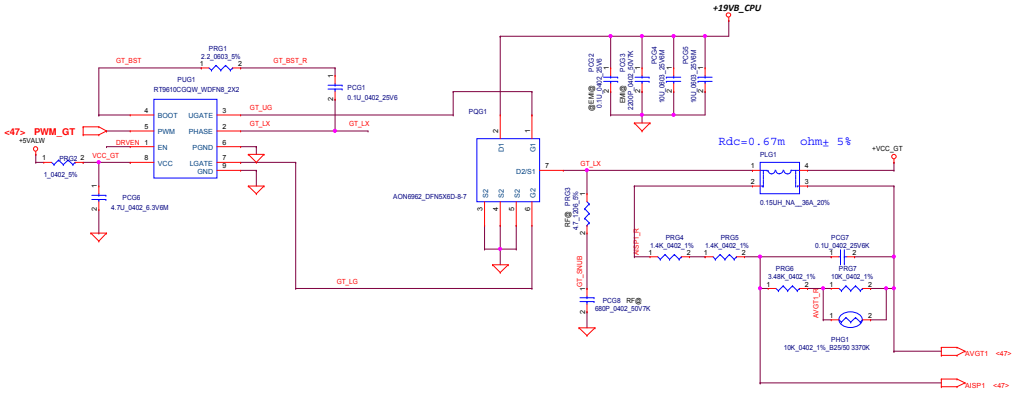
Title	CPU_CORE		
Size	Document Number	LA-H101P	Rev 0.A
Date:	Thursday, September 20, 2018	Sheet 47 of 54	





H/S AON6280:
R DS(ON) (at V GS =10V) < 6.8m
R DS(ON) (at V GS =4.5V) < 10.5m

L/S AON6214:
R DS(ON) (at V GS =10V) < 2.8m?
R DS(ON) (at V GS =4.5V) < 3.5m?



VCC_CORE
FSW=450kHz
Choke=0.15uH
DCR=0.67 mohm +/- 5%

U22
LL=2.4 mohm
TDC=21A
ICCMAX=32A
OCP=40A

U42
LL=2.4 mohm
TDC=42A
ICCMAX=64A
OCP=70A

VCC_GT
FSW=450kHz
Choke=0.15uH
DCR=0.67 mohm +/- 5%

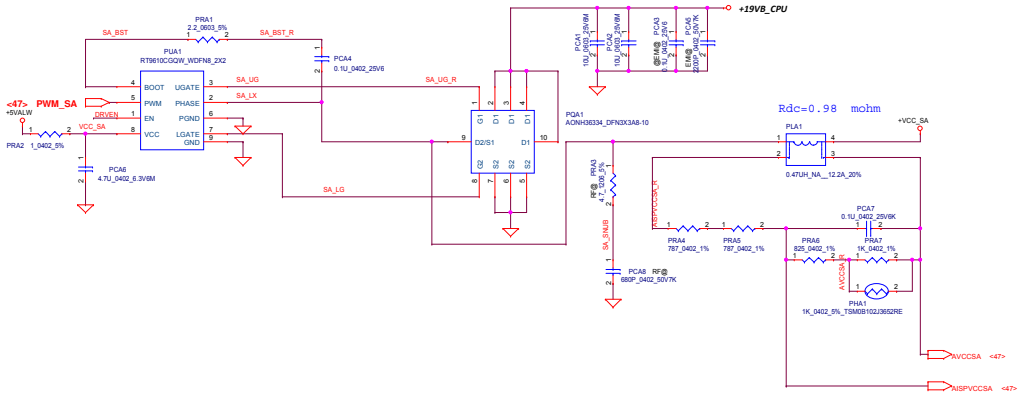
U22
LL=3.1 mohm
TDC=18A
ICCMAX=31A
OCP=39A

U42
LL=3.1 mohm
TDC=12A
ICCMAX=28A
OCP=39A

VCC_SA
FSW=600kHz
DCR=6.2 mohm +/- 5%

U22
LL=10.3 mohm
TDC=4A
ICCMAX=5A
OCP=10A

U42
LL=10.3 mohm
TDC=4A
ICCMAX=5A
OCP=10A



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2018/04/09	Deciphered Date	2019/04/09
Title	CPU Power stage		
Size	Document Number	LA-H101P	Rev 0.A
Date: Thursday, September 20, 2018	Sheet 48 of 54		

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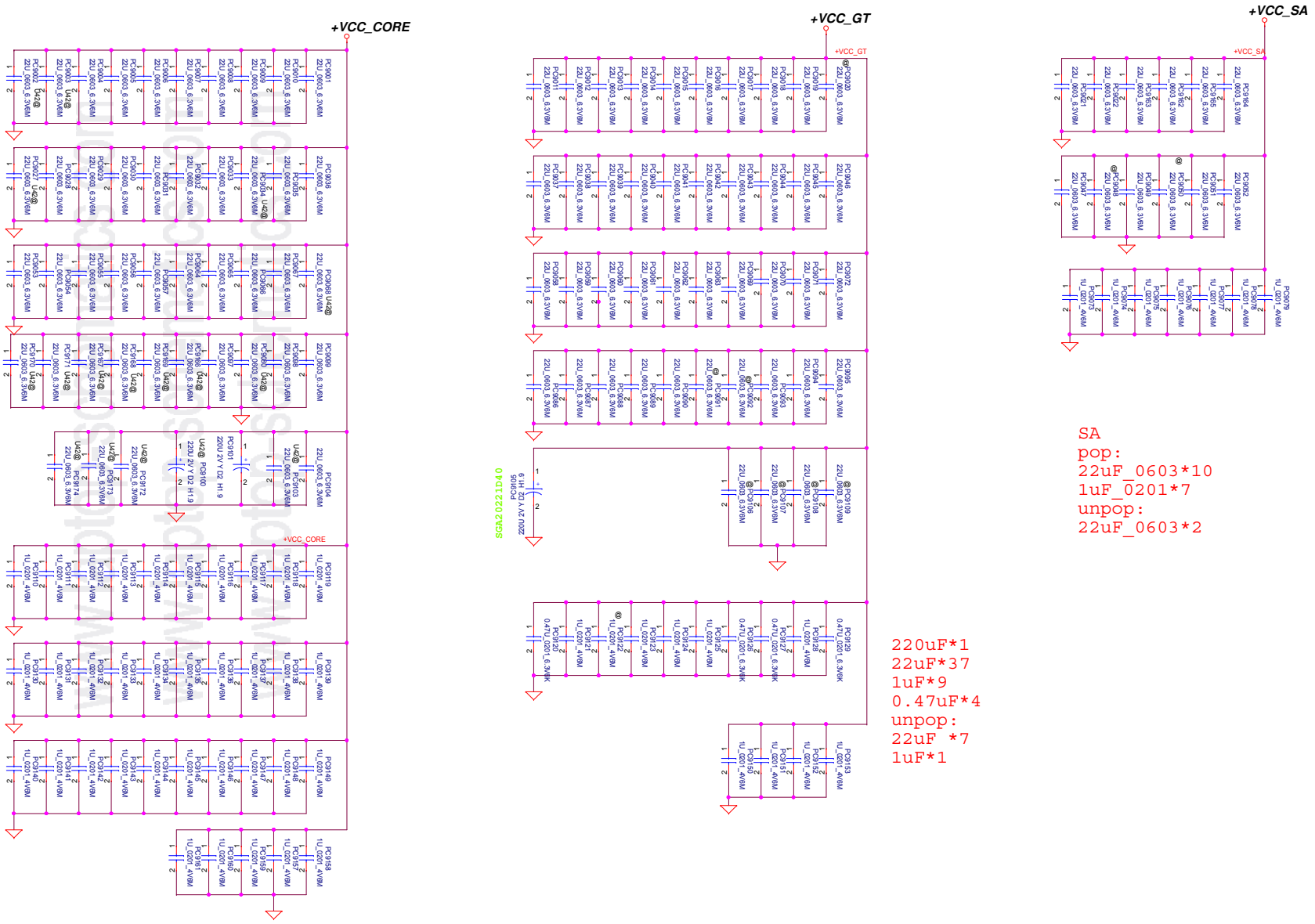

Security Classification	Compal Secret Data		
Issued Date	2018/10/10	Deciphered Date	2018/11/04

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Compal Electronics, Inc.

Title: Power Train

Size	Document Number	Rev
C	LA-H101P	0.A

Date: Thursday, September 20, 2018 Sheet 49 of 54

R1, R2, R3, R4, R5, C are based on VGA type to set.

OpenVReg Configurations:(PSI pin)

Operation phase Number	PSI Voltage setting
1 phase with DEM	0V to 0.4V
1 phase with CCM	0.7V to 0.88V
2 phase with DEM	1.08V to 1.35V
2 phase with CCM	1.6V to 5.5V

Module model information:
RT8816A-2P_NVVDDS_V2A.mdd for IC portion
RT8816A-2P_NVVDDS_V2B.mdd for SW portion

Vboot=Vvref*Rref2/(Rref1+Rref2+Rboot)
Rt=Rrefadj // (Rboot+Rref2)
Vmin= Vvref*[Rref2/(Rref2+Rboot)]*[Rt/(Rref1+Rt)]
Vmax=Vvref*Rref2/[(Rref1//Rrefadj)+Rboot+Rref2]
Vout=Vmin+N*Vstep
Vstep=(Vmax-Vmin)/Nmax

PSI pull up on HW side
+1.8VGS_+3VGS_AON

PWM VID and Output voltage control
1.Boot mode
2.Standby mode (don't support)
3.Normal mode

RT8816BGQW_WQFN20_3X3

Remark:
1. Switching frequency setting:(Ton pin)
Fsw=(Vin-0.5)/(2*Vin*Rton*3.2p)
=352Khz

Current Limit threshold setting
Rocset= (Ivalley * Rds(on) * 12) / Icoset

High: >1.2V
Low: <0.55V

N16S-GTR
+VGA_CORE
EDP-Continuous 26.5A
EDP-Peak 53A
OCP min 63.6A

N17S-G1
+VGA_CORE
EDP-Continuous 29.7A
EDP-Peak 59.2A
OCP min 71.1A

+VGA_CORE Near GPU Core

+VGA_CORE GB4-128 package Under GPU Core

Security Classification	Compal Secret Data		
Issued Date	2012/04/19	Deciphered Date	2015/04/19

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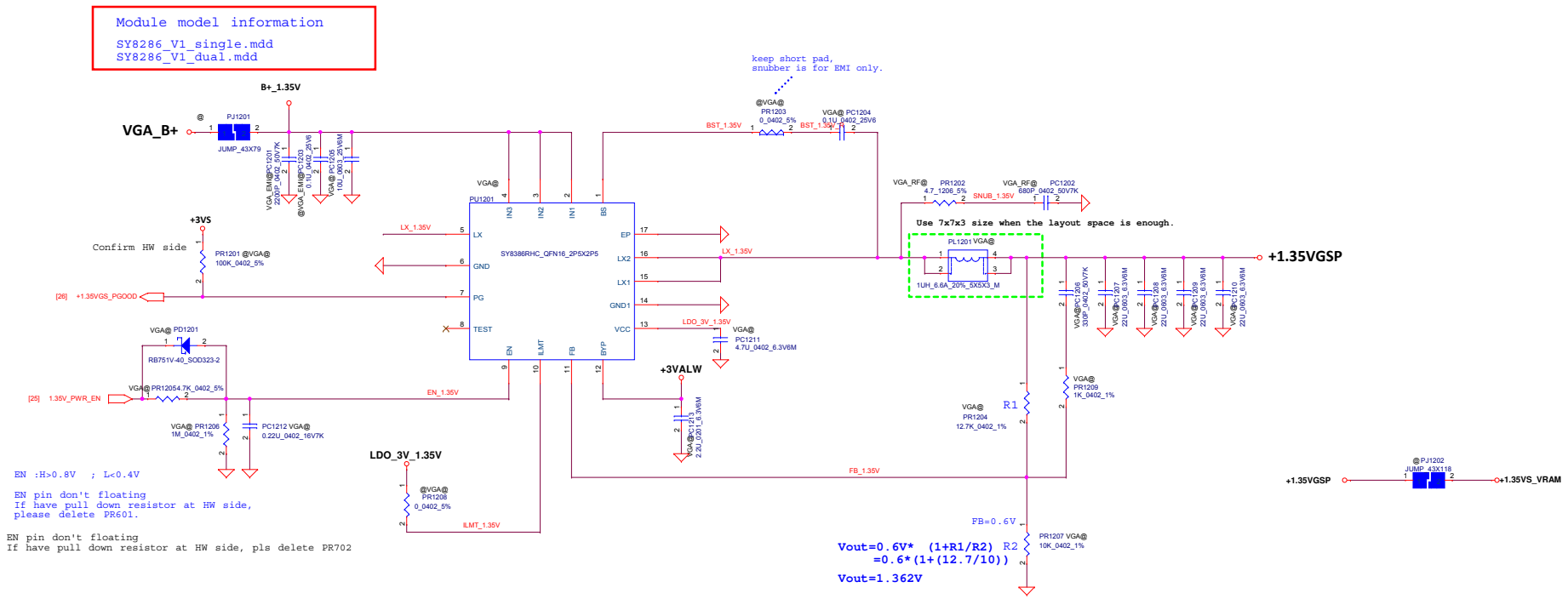
Compal Electronics, Inc.

Title: VGA_CORE

Size: Custom | Document Number: LA-H101P | Rev: 0.A

Date: Monday, October 22, 2018 | Sheet 50 of 53



Security Classification	Compal Secret Data		
Issued Date	2016/6/2	Deciphered Date	2017/6/2

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Compal Electronics, Inc.			
Title: VRAM-SY8286RAC			
Size: Custom	Document Number: LA-H101P		Rev: 0.A
Date: Monday, October 22, 2018	Sheet 51 of 53		

Version change list (P.I.R. List)

Item	Reason for change	PG#	Modify List	Date	Phase
1					
2					
3					
4					
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6					
7					
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10					
11					
12					
13					
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16					
17					
18					

Security Classification	Compal Secret Data		
Issued Date	2018/04/09	Deciphered Date	2019/04/09

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Compal Electronics, Inc.

Title: PIR (PWR)

Size	Document Number	Rev
Custom	LA-H101P	0.A

Date: Thursday, September 20, 2018 | Sheet 52 of 54

Version change list
(P.I.R. List)

Item		PG#	Modify List	Date	Phase
1					
2					
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Security Classification	Compal Secret Data		
Issued Date	2018/09/21	Deciphered Date	2019/09/21

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Compal Electronics, Inc.

Title: **PIR (HW)**

Size	Document Number	Rev
Custom	*LA-H101P*	0.6

Date: Thursday, September 20, 2018 | Sheet 53 of 51